ECG707: Logic Synthesis
Course Syllabus

Time and room: **F** 8:30-11:15 am.; Room: Aldec Lab.
Prerequisites: graduate standing
Textbook: Logic Synthesis, Srinivas Devadas et. Al., McGraw-Hill, 1994.
Instructor: Dr Henry Selvaraj
Office: TBE B-322 **Phone:** 895 4184 **Email:** henry.selvaraj@unlv.edu

Semester Grades will be computed as follows:

2 exams	200 points (75+125) (March 2 and April 13)
final exam/project	150 points
home work/projects	150 points
Total	500 points

All the examinations are closed book examinations. Final examination will be comprehensive.

Topics:
Programmable logic devises, design methodologies; design entries: truth tables, VHDL, BDDs, FSM, Blif; functional decomposition: partition algebra: strategies, serial decomposition, coding algorithms for encoding G functions; experiments with a serial decomposer; designs using PLA; parallel decomposition, argument reduction; introduction to FPGAs (Xilinx and Altera), maximum decomposition theorem, complete decomposition, logic synthesis using DECMAIN.
DAGs, BDDs, Ordered BBDs and Reduced Ordered BDDs. ROBDD implementation.
Finite State Machines (FSM), Decomposition of FSMs.
Technology Mapping, Technology libraries, cost models, graph covering and Technology mapping by Tree Covering.
On going works and future directions: network partitioning, synthesis for power.
Study of Xilinx devices, placement and routing issues and design using Xilinx FPGAs.
Study of Altera devices, Max+Plus II, designs using Altera FPGAs.
Group projects using Active VHDL, Espresso/Decmain/FPGA Express, and Xilinx/Max+PlusII.

- The course home page is located at: http://www.ee.unlv.edu/~selvaraj/
- Important announcements, notices and any other current information will be posted in the homepage.
- Homework will be due on the designated day at the start of class. No credit will be given for late homework. Homework solutions will be posted outside my office after due date. Homework problems will not be discussed in class. You are welcome to clear doubts in my office during office hours.
- Late homework will be accepted for full credit if and only if illness or truly urgent business interferes with the schedule of the course. Please make arrangements in advance.
- No make up test/exam will be given. If the student presents convincing evidence for his/her absence on the exam day, he/she will be allowed to take the final with an additional weight equal to that of the mixed exam.
- **As per University rules, drops and withdrawals will not be allowed after the due date even with instructor approval.**
- Attendance is required in class.
- Cheating: Students are encouraged to discuss problems with each other. However please do not copy homework. It is not going to help you in the long run.
- **Any person caught cheating will be given an `F' grade for the course and reported to appropriate university officials.**
- If you have a documented disability that may require assistance, you will need to contact the Disability Resource Center (DRC) for coordination in your academic accommodations. The DRC is located in the Reynolds Student Service Complex in room 137. The phone number is 895 0866 or TDD 895-0652. Or visit the DRC website at:
  http://www.nscee.edu/unlv/Student_Services/Disability_Resource_Center/
- It is UNLV's policy to give students who miss class because of observance of religious holidays the opportunity to make up missed work. Students are responsible for notifying the instructor of plans to observe the holiday.

Rules Regarding Homework
- Do not wait to finish the chapter to start your homework.
- All homework assignments are due in class at the beginning of class.
- Staple all your sheets together. I will not accept loose papers.

Henry Selvaraj
January 20, 2012