CPE100: Computer and Logic Design I
Course Syllabus - Fall 2014

Time and room: Section 3; MW 2:30 to 3:45 pm.
Prerequisites: MAT 126-127 or MAT 128 (Pre Calculus I and II) (GRADE C or above)
Textbook: Fundamentals of Logic Design, Charles H. Roth, Jr., VII edition, PWS Publishing Company.

Instructor: Dr Henry Selvaraj
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Semester Grades will be computed as follows:

Test 1:	20 points	(Sept. 29)
Test 2:	25 points	(October 27)
final exam:	35 points	
home work:	20 points	
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Total	100 points	

- The course home page is located at: http://www.ee.unlv.edu/~selvaraj/
- Important announcements, notices and any other current information will be posted in the homepage.
- Please read the course description in the home page.
- Homework will be due on the designated day at the start of class. No credit will be given for late homework. Homework solutions will be posted outside my office after due date. Homework problems will not be discussed in class. You are welcome to clear doubts in my office during office hours.
- Office Hours: MW 11:00 am. to 1:00 pm. If you are not able to make these times, call and make an appointment.
- Late homework will be accepted for full credit if and only if illness or truly urgent business interferes with the schedule of the course. Please make arrangements in advance.
- No make up test/exam will be given under any circumstances. If the student presents convincing evidence for his/her absence on the exam day, he/she will be allowed to take the final with an additional weight equal to that of the mixed exam.
- Last date to drop classes: October 31, 2014.
  As per the University rules, drops and withdrawals will not be allowed after this date even with instructor approval.
- Attendance is required in class.
- Cheating: Students are encouraged to discuss problems with each other. However please do not copy homework. It is not going to help you in the long run.
- **Any person caught cheating will be given an `F' grade for the course and reported to appropriate university officials.**
- If you have a documented disability that may require assistance, you will need to contact the Disability Resource Center (DRC) for coordination in your academic accommodations. The DRC is located in the Reynolds Student Service Complex in room 137. The phone number is 895 0866 or TDD 895-0652. Or visit the DRC website at:
  http://www.nscee.edu/unlv/Student_Services/Disability_Resource_Center/
- It is UNLV's policy to give students who miss class because of observance of religious holidays the opportunity to make up missed work. Students are responsible for notifying the instructor no later than the September 5) of plans to observe the holiday.

Rules Regarding Homework

- Do not wait to finish the chapter to start your homework.
- All homework assignments are due in class at the beginning of class.
- All problems must be started on a separate sheet and written neatly on 8.5 by 11 inch paper.
- Put a box around your final answer.
- Staple all your sheets together. I will not accept loose papers.

Topics:
Chapters 1-12 in the text book.

Henry Selvaraj
August 25, 2014.

CPE 100 – COMPUTER AND LOGIC DESIGN I: COURSE DESCRIPTION

CATALOG DATA
Digital design concepts and fundamentals. Combinational circuits. MSI and LSI circuits. Sequential machine fundamentals sequential circuit analysis and design. Modern developments.

COURSE OBJECTIVES
To gain the knowledge on
- number systems and binary arithmetic, basics of switching algebra, simplification and minimization methods for Boolean functions
- basic gates and simple integrated circuits that can be used for combinational network design
- different types of flip-flops, basics of sequential network design

TOPICS
- number systems and binary arithmetic
- basics of switching algebra
- simplification and minimization methods for Boolean functions
- AND, OR, NOT, NAND, NOR, EXOR gates as construction blocks for switching network design
- medium scale integrated circuits that can be used for combinational network design
- different types of flip-flops and their functionality
- basics of sequential networks design
- functionality of multiplexers, decoders, ROMs, PLAs, PALs

COURSE OUTCOMES
Upon completion of this course, students should be able to:
- convert between number systems and perform binary arithmetic operations
- simplify Boolean expressions and prove validity of equations
- analyze and design combinatorial networks using basic gates
- derive minterm and maxterm expansions for the functions given algebraically or by truth tables.
- design multi- and two-level NOR and NAND networks, including multi-output networks
- to design combinational networks using multiplexers, decoders and ROMs
- to construct timing diagrams for asynchronous and synchronous networks
- to design simple sequential circuits using flip-flops.