

A RDT-Based Interconnection Network for Scalable Network-on-Chip Designs

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Abstract

The interconnection network plays an important role in the performance and energy consumption of a Network-on-Chip (NoC) system. In this paper, we propose a RDT(2,2,1)/ α -based interconnection network for NoC designs. RDT(2,2,1)/ α is constructed by recursively overlaying 2-D diagonal meshes (torus). The number of layers needed for routing the links in RDT(2,2,1)/ α is shown to be bounded at 6, which is feasible to be implemented with current and future VLSI technologies. With the innovative diagonal structure and its simple rank assignment, RDT(2,2,1)/ α possesses the following features: recursive structure, smaller diameter and average distance, embedded mesh/torus topology, a constant node degree of 8, and robust routing schemes. These features make RDT(2,2,1)/ α a promising solution for the interconnection network of NoC designs satisfying the requirements for scalability, energy-efficiency, customizability, and fault-tolerance.

Key words: Network-on-Chip, interconnection network, torus, scalability, routing

1. Introduction

As shown on the International Technology Roadmap for Semiconductors (ITRS) [6], high-performance microprocessors are expected to contain up to one billion transistors by the year 2007 and over four billion transistors by 2013. This rapid advance in VLSI technologies will soon make it possible to integrate a large number of processing units interconnected through communication network on a single chip. The high performance and energy-efficiency brought by the distributed architecture make system-on-chip (SoC) designs promising for challenging design problems in the telecommunications, multimedia, and consumer electronic domains [1].

As a new paradigm of SoC, with a communication-centric design style, Network-on-Chip (NoC) [1] was proposed to meet the distinctive challenges of providing functionally correct, reliable operation of interacting SoC components. A NoC system is composed of a large number of processing units communicating to other units

across the interconnection network. Packets travel through the network by passing one or more hops between the source and destination tiles.

The design of a NoC system must address the following four problems.

- *Scalability:* In a NoC system, the interconnection network plays an important role in providing scalability to accommodate larger number of transistors and alleviate design productivity gap [4]. On-chip networks will likely use networks with lower dimensionality to keep wire lengths short [5]. However, the scalability of current proposed solutions, including honeycomb structure [3], 2-D mesh [8], and butterfly fat tree structure [9], is either insufficient or unexplored.
- *Energy-efficiency:* As pointed out in [4], a significant amount of power of a NoC system is consumed by its interconnection network. As a result, when designing a NoC system, power needs to be treated as a major design constraint [4].
- *Customizability:* The customization levels can be categorized in architectural, protocol, QoS [7][9][11], and hardware/software issues [4]. It is desirable to provide customizable NoC design in order to find the best compromise between the performance and the major design constraints, such as power and area, for a specific application.
- *Fault-tolerance:* The processing units and communication links are subject to failures. It is highly desirable to have a NoC design which can provide certain protection for system under node or link failures.

To address the aforementioned problems, we propose an interconnection network design for NoC based on the Recursive Diagonal Torus (RDT) structure [14], which was originally proposed to connect massively parallel computers. An RDT structure is constructed by recursively overlaying 2-D diagonal meshes (torus). RDT(n, R, m) is a class of RDT in which each node has links to form base torus (rank-0) and m upper tori (the maximum rank is R) with the cardinal number n . In this

study, we particularly consider $\text{RDT}(2,2,1)/\alpha$, one type of RDT with a special rank assignment. We show that the $\text{RDT}(2,2,1)/\alpha$ has the following advantages: 1) high scalability due to its recursive structure, 2) low power consumption due to its smaller diameter and average distance, 3) architectural customizability with its embedded mesh/torus topology, 4) fault-tolerance capability with a constant node degree of 8 and robust routing schemes. These features make $\text{RDT}(2,2,1)/\alpha$ a promising solution for the interconnection network of an NoC design.

The advanced features of $\text{RDT}(2,2,1)/\alpha$ are attributed to the innovative diagonal structure [14] and its simple rank assignment. The diagonal routing inside the $\text{RDT}(2,2,1)/\alpha$ is feasible with the emergence of the X-architecture [12]. In this paper, we show that the number of layers needed for laying out $\text{RDT}(2,2,1)/\alpha$ is bounded at 6, which is feasible with current and future VLSI technologies [6].

The rest of the paper is organized as follows. Section 2 provides a brief introduction of the $\text{RDT}(2,2,1)/\alpha$ structure. Section 3 presents the study of the number of layers needed for laying out $\text{RDT}(2,2,1)/\alpha$. Section 4 discusses the properties of a $\text{RDT}(2,2,1)/\alpha$ -based interconnection network. Section 5 summarizes the paper.

2. The $\text{RDT}(2,2,1)/\alpha$ Structure

2.1 Definitions of the RDT

Definition 1 (Base Torus). The *base torus* is a two-dimensional square array of nodes, each of which is numbered with a two-dimensional number as follows:

$$\begin{array}{cccc} (0, 0) & (1, 0) & (2, 0) & \dots & (N-1, 0) \\ (0, 1) & (1, 1) & (2, 1) & \dots & (N-1, 1) \\ (0, 2) & (1, 2) & (2, 2) & \dots & (N-1, 2) \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ (0, N-1) & (1, N-1) & (2, N-1) & \dots & (N-1, N-1) \end{array}$$

where $N = n^k$ and both n and k are natural numbers. The torus network is formed with four links between node (x, y) and its neighboring four nodes: $(\text{mod}(x \pm 1, N), y)$ and $(x, \text{mod}(y \pm 1, N))$. This base torus is also called *rank-0 torus*.

On the rank-0 torus, a new torus-like network (*rank-1 torus*) is formed by adding four links between node (x, y) and nodes $(x \pm n, y \pm n)$. The direction of the new torus-like network is at an angle of 45 degrees to the original torus. On the rank-1 torus, another torus-like network (*rank-2 torus*) can be formed by adding four links in the same manner. Similarly, a *rank-(r+1) torus* can be formed upon *rank-r torus*.

Definition 2 ($\text{RDT}(n, R, m)$). $\text{RDT}(n, R, m)$ is a class of networks in which each node has links to form base torus

(rank-0) and m upper tori (the maximum rank is R) with the cardinal number n .

According to this definition, the degree of the $\text{RDT}(n, R, m)$ is $4(m+1)$ [14].

Definition 3 (Perfect RDT). A network in which every node has links to form all possible upper rank tori (i.e. $\text{RDT}(n, R, R)$) is called a perfect RDT ($\text{PRDT}(n, R)$), where n is the cardinal number, and R is the maximum rank.

We refer a *perfect torus* as one that contains all links and no two links overlap. An *independent torus* on rank- i is one that does not have links to other tori on rank- i .

One of the upper rank torus is assigned to each node in the $\text{RDT}(n, R, m)$ after n , R , and m are set. Thus, the structure of the $\text{RDT}(n, R, m)$ also varies with different assignments for upper rank tori to each node. This assignment is called *torus assignment*.

2.2 The $\text{RDT}(2,2,1)/\alpha$ structure

In this paper, we consider a simple RDT structure, $\text{RDT}(2, 2, 1)/\alpha$ with its torus assignment shown in Fig. 1. In this assignment, each node has eight links, four for the base (rank-0) torus and four for rank-1 or rank-2 tori. Fig. 1 only shows part of these links.

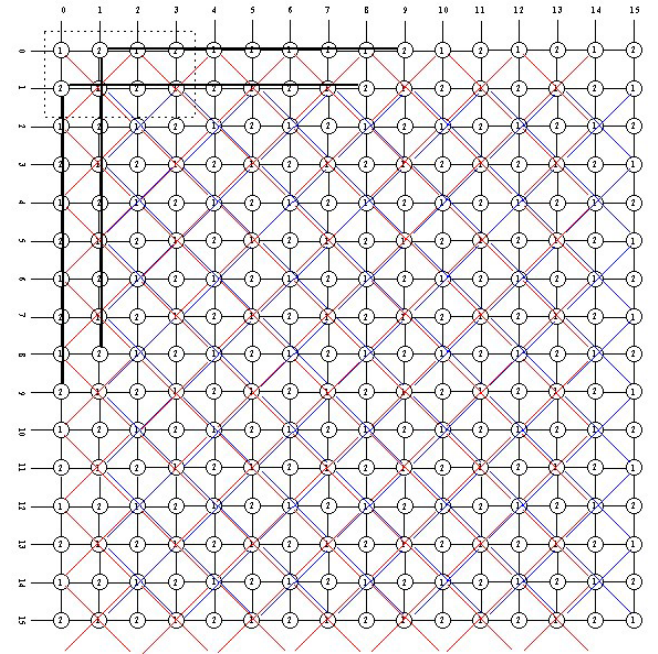


Figure 1. Torus assignment for the $\text{RDT}(2,2,1)/\alpha$.

According to Theorem 1 of [14], with the cardinal number $n=2$, eight independent rank-1 tori can be formed on the base torus, and eight independent rank-2 tori can be formed on each rank-1 torus. Hence, in total, there are 8 rank-1 tori and 64 rank-2 tori in $\text{RDT}(2,2,1)/\alpha$. As a perfect torus needs minimum 16 (4×4) nodes, a perfect $\text{RDT}(2,2,1)/\alpha$ consists of at least $64 \times 16 = 1024$ (32×32) nodes.

In $RDT(2,2,1)/\alpha$, we only use four independent rank-1 tori with their source nodes located at (0,0), (1,1), (2,0) and (3,1), respectively. Thirty-two rank-2 tori are formed on four rank-1 tori (1,0), (0,1), (2,1) and (3,0), respectively. Since the number of upper rank tori is only related to n , the number of independent rank-1 tori and the number of independent rank-2 tori remain the same irrespective of the size of base torus. Tab. 1 shows the source node (represented with rank-0 coordinate) of each independent rank- i torus, where $i=0, 1, 2$.

Table 1: Source node of each independent torus.

Rank	Source node
rank-0	(0, 0)
rank-1	(0, 0), (2, 0), (1, 1), (3, 1)
rank-2	(1, 0), (3, 0), (5, 0), (7, 0), (0, 1), (2, 1), (4, 1), (6, 1), (1, 2), (3, 2), (5, 2), (7, 2), (0, 3), (2, 3), (4, 3), (6, 3), (1, 4), (3, 4), (5, 4), (7, 4), (0, 5), (2, 5), (4, 5), (6, 5), (1, 6), (3, 6), (5, 6), (7, 6), (0, 7), (2, 7), (4, 7), (6, 7),

2.3 Routing algorithm

Compared with other $RDT(n, R, m)$ structures (such as $RDT(2, 4, 1)/\alpha$, $RDT(2, 4, 1)/\beta$ [14]), $RDT(2, 2, 1)/\alpha$ contains only the base torus and rank-1/2 tori. Due to its simpler structure, simplified versions of the vector routing algorithm and the floating vector routing algorithm [14] can be derived for $RDT(2, 2, 1)/\alpha$. We describe the floating vector routing algorithm as follows.

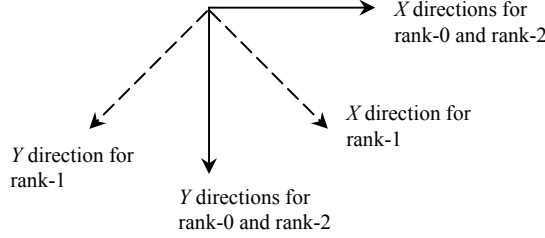


Figure 2. Directions of the coordinate.

On the torus structure, a vector from a source node to the destination node is represented with a vector $\vec{A} = a\vec{x}_0 + b\vec{y}_0$ where $\vec{x}_0$ and $\vec{y}_0$ are the unit vectors of the base (rank-0) torus. The goal of the routing algorithm is to represent vector $\vec{A}$ with a combination of vectors, each corresponding to a unit vector in one rank of the torus. Fig. 2 shows the directions of the unit vector for each rank torus, which rotate in clockwise direction at an angle of 45 degrees as the rank increases.

2.4 Diameter and average distance

Theorem 1 [15] The diameter of $PRDT(2,2)$ with the Vector Routing Algorithm [14] is:

$$D = \frac{N 2^{\lceil \frac{R-1}{2} \rceil}}{(2n)^R} + nR - 1$$

where N is the size of the base torus (the number of nodes is $N \times N$).

Based on the floating vector routing algorithm for $RDT(2,2,1)/\alpha$, we can show that the diameter of $RDT(2, 2, 1)/\alpha$ is the same as the diameter of $PRDT(2,2)$. Hence, the diameter of $RDT(2,2,1)/\alpha$ is given by $D = N/8 + 3$ for $n = 2$ and $R = 2$. Tab. 2 shows the diameters and average distances of $RDT(2, 2, 1)/\alpha$ for different network sizes following the floating vector routing. One can check that the diameter and average distances of $RDT(2,2,1)/\alpha$ are smaller than those of other parallel architectures, such as 2D Torus, 3D Torus, and Hypercube, with the same network size [2].

Table 2: Diameters and average distances of $RDT(2, 2, 1)/\alpha$.

Number of nodes	Diameter	Average distance
1024	7	4.31543
4096	11	6.32495
16384	19	10.3273

3. The $RDT(2,2,1)/\alpha$ -Based Interconnection Network for NoC

Due to its simple structure and high performance, $RDT(2,2,1)/\alpha$ is very suitable for interconnecting the processing units in an NoC. The emergence of the X-architecture makes it possible to perform diagonal routing. In this section, we study the feasibility of laying out $RDT(2,2,1)/\alpha$ with current and future VLSI technologies.

3.1 Links of $RDT(2,2,1)/\alpha$

Definition 4 (Link). A *link* is an edge which connects two nodes.

If two links intersect at a point which is not any end of each link, the two links are *jump crossing*. As we know, in circuit design, two jump crossing links cannot be laid out on the same layer. Assuming that all the processing units (represented as nodes in $RDT(2, 2, 1)/\alpha$) are on the same layer, the objective of our study is to show that all links in $RDT(2, 2, 1)/\alpha$ can be laid out on a small number of layers.

Tab. 3 shows the source node and the destination node (be represented with rank-0 coordinate) of each link on each rank for a square array with $N \times N$ nodes. We categorize the links into 12 groups for $RDT(2, 2, 1)/\alpha$ with its base torus size set as $N \times N$. Tab. 4 describes the links on each rank. The first column shows the group no. (#); the second column shows the rank (R) and direction (D); the fifth column shows the length of links in each group normalized against the shortest link and the number of links in each group; the last column shows the number of groups (NG) in an $RDT(2, 2, 1)/\alpha$.

Table 3. Links on each rank.

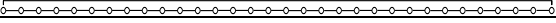
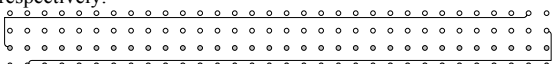
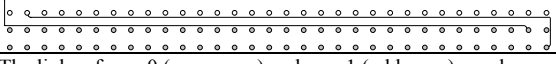
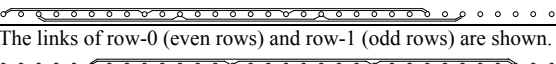
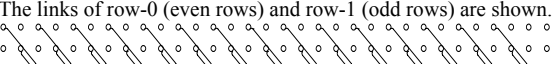
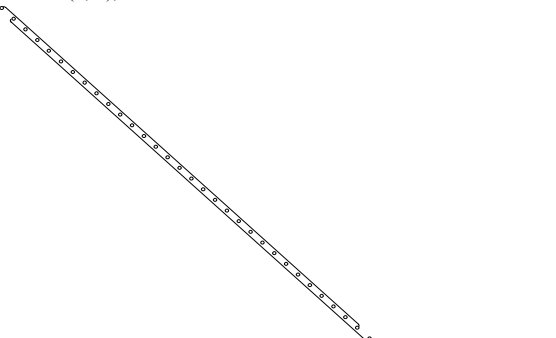
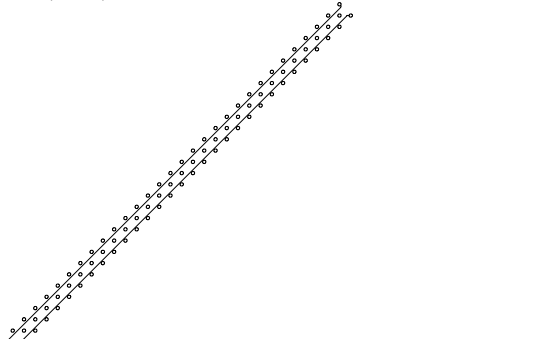
Source node	rank- i	Destination node of X direction for rank- i	Destination node of Y direction for rank- i
(x, y)	0	$((x+1) \bmod N, y)$	$(x, (y+1) \bmod N)$
(x, y)	1	$((x+2) \bmod N, (y+2) \bmod N)$	$((x-2) \bmod N, (y+2) \bmod N)$
(x, y)	2	$((x+8) \bmod N, y)$	$(x, (y+8) \bmod N)$

Table 4. Description of links.

#	R D	Source nodes of each independent torus	Linking method	Links		NG
				Len.	Num. of Links	
1	0 X	(0, 0)	$(x, y) \leftrightarrow ((x+1) \bmod N, y)$	1 $N-1$	$N-1$ 1	N
2	0 Y	(0, 0)	$(x, y) \leftrightarrow (x, (y+1) \bmod n)$	1 $N-1$	$N-1$ 1	N
3	1 X	(0,0), (2,1), (1,1), (3,1)	$(x, y) \leftrightarrow ((x+2) \bmod N, (y+2) \bmod n)$	$2\sqrt{2}$ $(N-2)$ $\sqrt{2}$	$N-2$ 2	$N/4$ 1
4	1 X	(0,0), (2,1), (1,1), (3,1) Links between $(i, N-2)$ and $(i+2, 0)$, where $i=0, 2, \dots, N-4$ and links between $(i, N-1)$ and $(i+2, 1)$, where $i=1, 3, \dots, N-3$.	$(x, y) \leftrightarrow ((x+2) \bmod N, (y+2) \bmod n)$	N	2	$(N-2)/2$
5	1 X	(0,0), (2,1), (1,1), (3,1) Links between $(N-2, i)$ and $(0, i+2)$, where $i=0, 2, \dots, N-4$ and links between $(N-1, i)$ and $(1, i+2)$, where $i=1, 3, \dots, N-3$.	$(x, y) \leftrightarrow ((x+2) \bmod N, (y+2) \bmod n)$	N	2	$(N-2)/2$
6	1 Y	(0, 0), (2, 0), (1, 1), (3, 1)	$(x, y) \leftrightarrow ((x-2) \bmod N, (y+2) \bmod n)$	$2\sqrt{2}$ $(N-2)$ $\sqrt{2}$	$N-2$ 2	$N/4$ 1
7	1 Y	(0, 0), (2, 0), (1, 1), (3, 1) Links between $(i, N-2)$ and $(i-2, 0)$, where $i=2, 4, \dots, N-2$ and links between $(i, N-1)$ and $(i-2, 1)$, where $i=3, 5, \dots, N-1$.	$(x, y) \leftrightarrow ((x-2) \bmod N, (y+2) \bmod n)$	N	2	$(N-2)/2$
8	1 Y	(0, 0), (2, 0), (1, 1), (3, 1) Links between $(N-2, i)$ and $(0, i-2)$, where $i=4, 6, \dots, N-2$. A set of links linking nodes $(N-1, i)$ and $(1, i-2)$, where $i=3, 5, \dots, N-1$.	$(x, y) \leftrightarrow ((x-2) \bmod N, (y+2) \bmod n)$	N	2	$(N-2)/2$
9	2 X	(1,0), (3,0), (0,1), (2,1), (1,2), (3,2), (0,3), (2,3), (1,4), (3,4), (0,5), (2,5), (1,6), (3,6), (0,7), (2,7)	$(x, y) \leftrightarrow ((x+8) \bmod N, y)$	8 24	$(N/8-1)*2$ 2	$N/2$
10	2 X	(5,0), (7,0), (4,1), (6,1), (5,2), (7,2), (4,3), (6,3), (5,4), (7,4), (4,5), (6,5), (5,6), (7,6), (4,7), (6,7)	$(x, y) \leftrightarrow ((x+8) \bmod N, y)$	8 24	$(N/8-1)*2$ 2	$N/2$
11	2 Y	(0,1), (0,3), (1,0), (1,2), (2,1), (2,3), (3,0), (3,2), (4,1), (4,3), (5,0), (5,2), (6,1), (6,3), (7,0), (7,2)	$(x, y) \leftrightarrow (x, (y+8) \bmod N)$	8 24	$(N/8-1)*2$ 2	$N/2$
12	2	(0,5), (0,7), (1,4), (1,6),	$(x, y) \leftrightarrow (x, (y+8) \bmod N)$	8	$(N/8-1)*2$	$N/2$

Y	(2,5), (2,7), (3,4), (3,6), (4,5), (4,7), (5,6), (6,5), (6,7), (7,4), (7,6)	$+ 8) \bmod N)$	24	2	
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For clarity, Fig. 3 shows the links used in each group for RDT(2, 2,1)/ α with base torus $N=32$ (i.e., $32 \times 32 = 1024$ nodes).

#	Links
1	The same links are used in 32 rows. 
5	The links of row-0 and row-1 are shown. The links of even rows and odd rows are the same as those of row-0 and row-1 respectively. 
8	The links of row-0 (even rows) and row-1 (odd rows) are shown. 
9	The links of row-0 (even rows) and row-1 (odd rows) are shown. 
10	The links of row-0 (even rows) and row-1 (odd rows) are shown. 
3	The links of row-0 (even rows) and row-1 (odd rows) are shown. Links from node $(n-2, n-2)$ to node $(0, 0)$ and from node $(n-1, n-1)$ to node $(1, 1)$, where $n=32$. 
6	The links of row-0 (even rows) and row-1 (odd rows) are shown. Links from node $(0, n-2)$ to node $(n-2, 0)$ and from node $(1, n-1)$ to node $(n-1, 1)$, where $n=32$. 

#	Links	#	Links	#	Links	#	Links	#	Links
2		4		7		11		12	
The same links are used in 32 columns.		The links of column-0 and column-1 from left to right in each group are shown. The links of even columns are the same as that of column-0. The links of odd rows are the same as that of column-1.							

Figure 3. The links described in Table 4 with $N=32$.

3.2 Layers of $\text{RDT}(2,2,1)/\alpha$

From Fig. 3, it can be seen that links on different directions are deemed to be jump crossing. According to the direction of these links, we can classify the groups in Fig. 3 into four sets.

Set 1 (Horizontal): Groups 1, 5, 8, 9, and 10

Set 2 (Vertical): Groups 2, 4, 7, 11, and 12

Set 3 (45 degree): Group 3

Set 4 (135 degree): Group 6

The links in groups 5, 9, 4 and 11 are jump crossing with the links in groups 8, 10, 7 and 12, respectively. So set 1 has to be divided into 2 sub-sets:

Set 1-1: Groups 1, 5, and 9

Set 1-2: Groups 8 and 10.

Set 2 is also divided into 2 sub-sets:

Set 2-1: Groups 2, 4, and 11

Set 2-2: Groups 7 and 12.

As a result, the routing of $\text{RDT}(2,2,1)/\alpha$ needs 6 layers:

Layer 1: 1, 5, 9

Layer 2: 8, 10

Layer 3: 2, 4, 11

Layer 4: 7, 12

Layer 5: 3

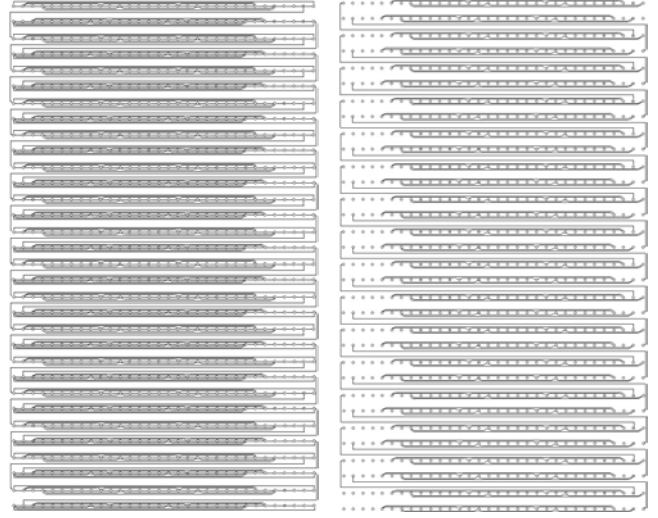
Layer 6: 6

Fig. 4 shows the links at each layer of an $\text{RDT}(2,2,1)/\alpha$ with its base torus size $N=32$.

Now we show 6 layers are also necessary for laying all links without any concern for jump crossing. Layer 1 cannot be combined with any other layer since links in group 1 are jump crossing with links in groups 8, 11, 12, 3, and 6, respectively. Similarly, we can show that layer 2 to layer 6 cannot be combined with the other five layers for the problem of jump crossing links otherwise would be incurred. Hence, we have the following theorem.

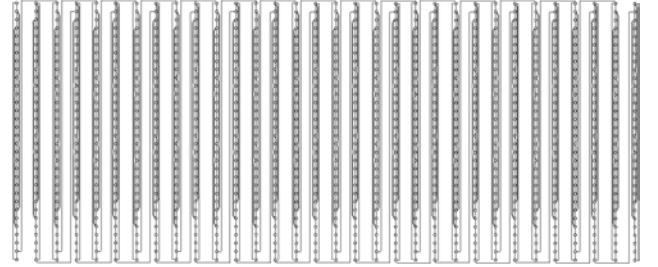
Theorem 2: The least number of layers needed for laying

out $\text{RDT}(2,2,1)/\alpha$ is 6.

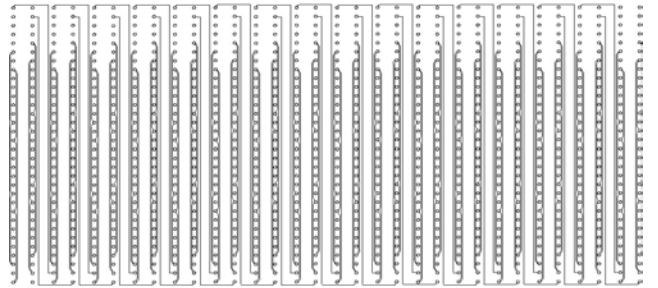


(a) Links on layer 1.

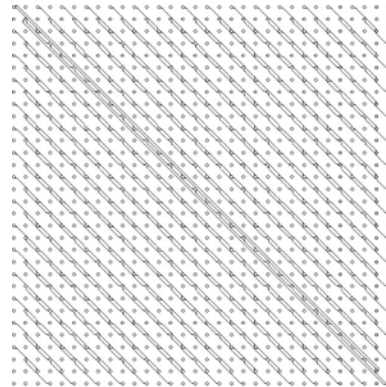
(b) Links on layer 2.



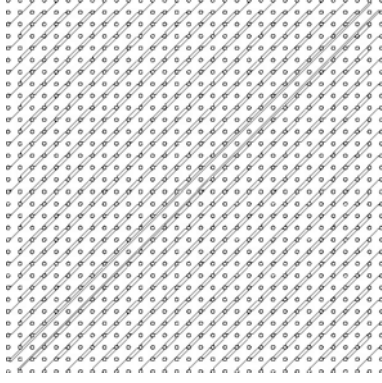
(c) Links on layer 3.



(d) Links on layer 4.



(e) Links on layer 5.



(f) Links on layer 6.

Figure 4. The links on each layer of RDT(2,2,1)/α with base torus size $N=32$.

With current and future VLSI technologies [6], 6 or more layers are available for signal routing. Tab. 5 summarizes the length of lines on each layer of the layout.

Table 5: Total length of links on each layer.

Layer	Total length of links	$N = 1024$	$N = 4096$	$N = 16384$
1	$3N^2 - 3N/2 + 32$	3M	50M	805M
2	$N^2 + N/2 + 32$	1M	16M	268M
3	$3N^2 - 3N/2 + 32$	3M	50M	805M
4	$N^2 + N/2 + 32$	1M	16M	268M
5	$\sqrt{2} N^2 + \sqrt{2} N - 4\sqrt{2}$	1M	23M	379M
6	$\sqrt{2} N^2 + \sqrt{2} N - 4\sqrt{2}$	1M	23M	379M

4. Properties of the RDT(2,2,1)/α-Based Interconnection Network

The RDT(2,2,1)/α-based interconnection network has the following properties.

Property 1: it is highly scalable. This property follows from definition of RDT(2,2,1)/α and the method of link grouping in RDT(2,2,1)/α. It is worthy to point out that the number of independent tori and the number of link groups of RDT(2,2,1)/α are not changing with the size of the network. The method of link grouping is easy to follow since it considers both the rank and the direction that each link falls into.

Property 2: the energy consumption due to communication tends to be low as a direct result of its small diameter and average distance (as shown in Table 1). As one can see from Table 5, the total length of lines on each layer tends to be balanced.

Property 3: RDT(2,2,1)/α can be easily customized to simpler structure with the embedded torus/mesh topology.

Property 4: with the degree of 8 and robust routing scheme, RDT(2,2,1)/α provides fault tolerance inherently.

5. Summary

In this paper, we proposed a RDT(2,2,1)/α-based interconnection network for scalable NoC designs. We first introduced the RDT(2,2,1)/α structure which is constructed by overlaying 2-D diagonal meshes (torus). RDT(2,2,1)/α has a constant node degree of 8, and small diameter and average distance. With a special rank assignment, RDT(2,2,1)/α has simpler structure and routing scheme than other RDT structures, making it suitable for interconnecting processor units for NoC designs. We show that the interconnection network based on RDT(2,2,1)/α can be laid out with 6 layers, which is feasible with current VLSI technologies. Future study topics include the algorithm and compiler design for the RDT(2,2,1)/α-based NoC designs and the reconfigurability of RDT(2,2,1)/α structure.

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