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# Silicon photonic network-on-chip and enabling components

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As the transistor's feature scales down and the integration density of the monolithic circuit increases continuously, the traditional metal interconnects face significant performance limitation to meet the stringent demands of high-speed, low-power and low-latency data transmission for on- and off-chip communications. Optical technology is poised to resolve these problems. Due to the complementary metal-oxide-semiconductor (CMOS) compatible process, silicon photonics is the leading candidate technology. Silicon photonic devices and networks have been improved dramatically in recent years, with a notable increase in bandwidth from the megahertz to the multi-gigahertz regime in just over half a decade. This paper reviews the recent developments in silicon photonics for optical interconnects and summarizes the work of our laboratory in this research field.

**interconnects, optical technology, complementary metal-oxide-semiconductor (CMOS), silicon photonics**

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## 1 Introduction

In 1965, Gordon Moore, co-founder of Intel, first noted that the number of transistors per square inch on integrated circuits had doubled every year since the integrated circuit was invented in 1959. It became known later as Moore's law. The period often quoted as "18 months" is due to David House, the Intel executive, who predicted that period for a doubling in chip performance. Fabricating smaller devices on large wafers will increase the yield, reduce the cost and get faster circuits. So in the last 40 years, the dramatically scaling down of the complementary metal-oxide-semiconductor (CMOS) transistor has been the main driving force of the microelectronics industry illustrated by the Moore's law. However, the microelectronics and information industry realize that the end of the Moore's law is on the horizon because of several physical limits [1]. The most problematic bottleneck of which is the traditional metal interconnects [2–5]. Now in the market, a lot of integrated circuit (IC) products are based on the CMOS transistor with 45 nm feature sizes. In the near future, as the feature size scales down further, the COMS transistors will be fast enough to operate at clock speeds of 15 GHz [6]. But, as the metal wires scale down, the resistance-capacitance (RC) product of the interconnect wires increases, which increases the time delay and crosstalk (CT) of signals, and finally leads the power consumption to increase and limits the computing speed of IC.

Obviously, new interconnection technology is needed to overcome the limitations of traditional metal interconnects. The most promising candidate is to use optical interconnects. In fact, optical interconnects (OI), composed of single fre-

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quency lasers, fiber optics, fast detectors and wavelength division multiplexing (WDM) systems, have been used for decades in long-distance telecommunications. If the same approach is transplanted into the short-distance communications (e. g. on- and off-chip communications), it will increase the bandwidth, lower the latency and reduce the power consumption [7, 8]. Nowadays, most commercial photonic devices are made by III-V group materials such as InP and GaAs, which make them hard to integrate with silicon-based IC, and consequently, expensive. The silicon-on-insulator (SOI) structure provides a natural planar optical waveguide with a refractive index at 1550 nm of approximately 3.5 and 1.46 for silicon (Si) and $SiO_2$. Such high refractive index difference of sub-micron waveguides provides strong optical confinement and thus permits waveguides with small bend radii. This benefits reducing the devices' footprint and increasing the integration dense. In addition, for optical wavelengths longer than 1100 nm, both Si and $SiO_2$ are transparent, thus optical loss and power dissipation are negligible. Hence Si photonics is an ideal candidate for next-generation optical networks on chips (ONoCs) because of its compatibility with the CMOS technology, which makes it possible to fabricate optoelectronic chip monolithically with a cost-effective engineering [9].

Due to researchers' active contributions, Si fundamental building-block photonic devices of an optical transmission link, such as optical sources, modulators, switches (routers) and detectors, have been improved dramatically in recent years, with a notable increase in bandwidth from the megahertz to the multi-gigahertz regime in just over half a decade. Several optical network architectures based on such devices are also proposed. This paper reviews the recent developments in Si photonics for optical interconnects and summarizes the work of our laboratory in this research field.

## 2 Photonic network-on-chip (PNoC) architecture

### 2.1 PNoC proposed by other research groups

As PNoC is an attractive option to break the bottleneck of electronic interconnects, its architectures and network topologies for data transmission with ultra-large bandwidth and low power consumption are developed by many different groups to meet the critical requirement in future high performance IC, such as chip multiprocessors (CMPs) [10–17].

Hewlett-Packard (HP) Laboratories and their collaborators proposed Corona, a system that contains 64 clusters and each cluster has 4 cores. In this architecture, intercore and off-stack communication are both implemented by on-chip optical components. The 64 clusters communicate through an optical crossbar and occasionally an optical broadcast ring. For the sake of resolving the optical signal conflict in the crossbar and broadcast bus, optically activated arbitration schemes are designed [10]. Their later study shows that if the dense wavelength division multiplexing (DWDM) is considered in the optical interconnects, the system's computing performance will be improve greatly [11, 12].

Kirman et al. [13] explored a hierarchical optoelectronic bus architecture, which accommodates 64 four-issue out-of-order cores. The PNoC is directly borrowed from the electrical baseline address and data networks. Several possible bus topologies, with a range of 4 to 12 available wavelengths per waveguide, are investigated. Results show that the proposed bus achieves significant performance improvement for high-bandwidth applications compared to a state-of-the-art fully electrical bus. It is also stated that the system performance can be further developed if the degree of the electronic interconnects replaced by photonic interconnects increases.

Bergman's group proposed a 3D integration (3DI) hybrid architecture including a folded-torus topology PNoC at the top layer [14]. The optical modulators and detectors, which realize the electro-optic (EO) and opti-electronic (OE) conversion, are connected to the multicore layer by using the through silicon via (TSV) technique. The WDM transmission scheme is employed to enable high bandwidth. They simulated the networks using a physical-layer simulator called PhoenixSim, which is developed by them in the OMNeT++ simulation environment, to measure the insertion loss, CT, and power [15].

It is not difficult to find that there are two communication styles of optical signals between different access points in the proposed network architectures. One is the use of wavelength-selective routing to directly guide messages from source to destination [10–13]. The other one is the space-switched system routing optical messages by utilizing active switches [14, 15]. However, the existing space-switched systems need an additional electronic control network to set up, release, and control the optical circuits (aka light paths). Separation of the optical and electronic control layer increases significant latency, power consumption and integration complexity.

### 2.2 Our proposed PNoC

We proposed a novel circuit-switched on chip photonic interconnection network (CSPIN) architecture that employs optical signals rather than electric signals to control the circuit switching functions [18]. The proposed CSPIN consists of two layers: the computation layer and the photonic layer. The computation layer is composed of the processing cores organized in clusters and local communication facilities. The photonic layer consists of the photonic interconnection network built with waveguides and optical routers. The CSPIN depicted in Figure 1(a) is composed of 64 nodes organized in 16 clusters which are interconnected by a 4×4 optical mesh. Inside a cluster, the four nodes are connected

by an electronic router, which is connected to an optical router. In CSPIN, communication between source and destination clusters includes four phases: i) Circuit setup (CS). In this phase, the source node sends the header slices containing the routing information to the destination node. Once receiving the header slices, each intermediate node will check if the output channel is available and reserves it or rejects the circuit setup request. When the destination node reserves the channel, a light path is built from the source node to the destination node. ii) Circuit confirmation (CC). In case that an intermediate node or the destination node has no channel to allocate, the CC will be fed back from the node to the downstream intermediate nodes and the source node. iii) Data payload (DP). If the light path is successfully established, the source node will transmit the DP to the destination node through the light path. iv) Circuit release (CR). After the DP process is finished, the destination node will return information to all the upstream nodes on the light path to release the reserved channel. Two schematic light paths with 3 and 4 hops are shown in Figure 1(a). They will be released after data transmission is accomplished.

The key component in the photonic layer is the optical router. Figure 1(b) shows our conceptual structure diagram of it. The transceiver units (TU) and reversing units (RU) both have 4 waveguides to connect the adjacent 4 optical routers. If the node is the source node, the electric data from the local core will be transmitted to the routing control units (RCU), which then manipulate the TU to send the data out with optical signals. Otherwise there are two conditions of the node: the intermediate node and destination node. In the case of the intermediate node, optical signals are launched into the RU. When there is channel available, the CS signals transfer to the detecting units (DU), and then the RCU. The RCU turn the RU to a "busy" state to tell other nodes that this channel has been requisitioned, meanwhile the RCU open the taps (optical switches) in the optical switching units (OSU) to build up the light path in this node. In the other case, if no channel is available, the CS signals will feed back to the upstream node through the RU. If this happens, the upstream node needs to retry to find an available light path. The function of the feedback units (FU) is to receive the feedback signals from the downstream node. The only difference between the destination and intermediate nodes is whether optical signals from the DU are directly converted to electric signals, and next, sent to the destina-

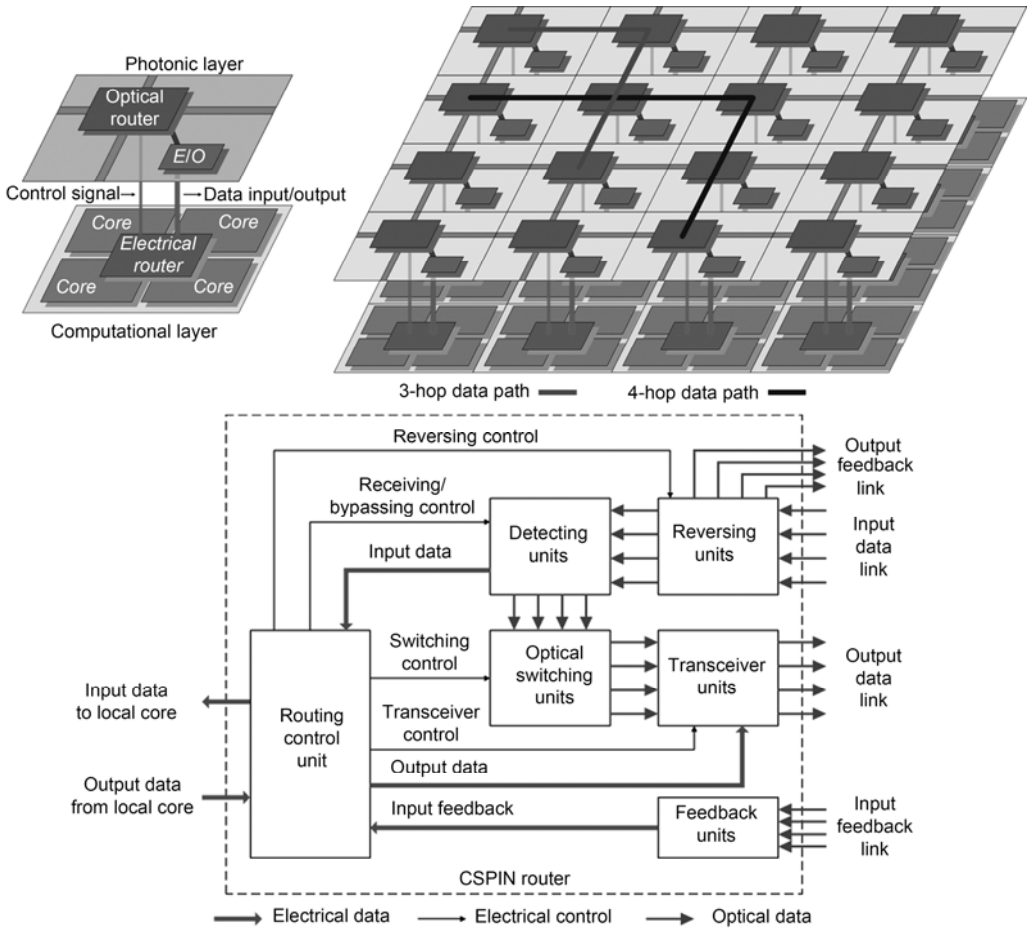


**Figure 1** (a) Illustration of CSPIN; (b) structure of a 4-channel CSPIN router [18].

tion local core via the RCU. As confirmed by the analysis, the CSPIN significantly reduces the power consumption and latency of the circuit-setup phase. In addition, it can help reduce the integration complexity of the on-chip interconnection network. Except the RCU constructed by electric circuit, the RU, TU and FU are realized by photonic components [18], which will be discussed in the next section.

## 3 Silicon photonic components for PNoC

In order to implement Si optical link between different access points, researchers explore many passive and active Si optical devices. By utilizing nanoscale lithographic techniques, passive devices based on sub-micron Si waveguides, such as filters [19−22], directional couplers [23, 24], multi-mode interferometers (MMIs) [25, 26], Mach-Zehnder interferometers (MZIs) [27, 28], arrayed waveguide gratings (AWGs) [29, 30], and photonic crystal devices [31−34], have been demonstrated.

For a long time, Si has not been considered as an optical material because it lacks the commonly used physical effects such as the electro-optic effect and stimulated emission. These effects are either nonexistent or extremely weak in Si. However, study finds that the stimulated Raman scattering (SRS) and free carrier dispersion (FCD) effects are strong in Si [35], which make active devices for optical amplification, lasing and modulating possible in Si. Rong et al. [36] demonstrated a kind of Raman Si laser based on a ring-resonator-cavity in 2007, which dramatically decreased the threshold pump power to 20 mW. The first Ge-on-Si laser operating at room temperature was reported in 2010, smartly using the pseudodirect gap properties of Ge [37]. In the past decade, optical modulators and detectors were improved dramatically toward to high-speed, low power and small footprint. Si optical modulator with a speed >10 Gbps has been demonstrated by many research groups [38−46]. The minimum energy consumption per bit of those modulators has been decreased below 100 fJ/bit. More recently, the extremely small modulator consisting of Si and metal with a length of only 4 μm has been made by Zhu et al. [47]. As the epitaxial technique of germanium on Si became mature, Ge-on-Si photo detectors reaching 30 GHz have been demonstrated by a lot of groups [48−52]. Another future look may lie on the graphene-silicon photo detectors [53]. In future, it is hopefully to see the devices with bandwidth larger than 500 GHz and quite low cost. Multichannel detection can probably be another supporting.

To implement the optical link in our proposed CSPIN, we designed and fabricated relative Si photonic components that may be used to build the OSU, RU, TU and FU of the optical router in the photonic layer on SOI platform by the CMOS-compatible process. Measurements are also carried out to characterize the properties of the fabricated devices. This section summarizes the recent experimental work on Si optical devices of our research group.

### 3.1 Si MRR-based optical add-drop filters

Microring resonators (MRRs) are versatile elements widely used for various applications, including filters [54], modulators [38], switches [55, 56], and sensors [57]. The basic add-drop filter function of MRRs can be used to compose passive wavelength-routed networks (e.g. crossbars) [58−60]. Actually, the OSU in our proposed CSPIN router is a 4×4 optical crossbar switch. The RU, DU, FU and TU can be realized by the EO-tuned MRRs and photo detectors [18]. Hence we start with the filter characteristics of MRRs.

Figures 2(a)−2(c) show the pictures of the 1st-, 2nd- and 3rd-order MRR filters [61, 62], which are fabricated on an 8 inch SOI wafer with a 220-nm-thick top Si layer and a 2-μm-thick buried dioxide layer. The 248 nm deep ultraviolet (UV) photolithography is used to define the device pattern. The inductively coupled plasma etching process is used to etch the top Si layer. Rib waveguides with a cross section of 450 nm × 220 nm and a 60-nm-thick slab are adopted. The gaps (Gap1) between bus waveguides and ring waveguides are all designed with 200 nm. And the gaps (Gap2) between ring and ring waveguides are designed to be 450 nm and 440 nm in the 2nd- and 3rd-order MRR filters, respectively. Grating couplers, as shown in Figure 2(d), are integrated to couple light into and out of devices. For the 3rd-order MRR filter, a 120-nm-thick TiN is sputtered on the 1.5-nm-thick $SiO_2$ cover layer. The TiN heaters are fabricated by UV photolithography and dry etching to compensate the resonances shift of MRRs caused by fabrication errors (through thermo-optical (TO) effect). The 10-μm-wide aluminum wires connect the TiN heaters to the 100 μm × 100 μm pads.

The measured optical response spectra are shown in Figures 2(e)–2(g). As seen from the figures, for the 10-μm-radius 1st-order MRR filter, the extinction ratio (ER) of the through port (TP) and drop port (DP) are around 20 dB. The free spectral range (FSR) is about 10 nm. Usually, box-like response is preferred to improve the filter's performance. Figure 2(f) shows the response spectra of the 5-μm-radius 2nd-order MRR filter. One can see that, though box-like response spectra with high ER (much higher than that of the 1st-order MRR filter) at the drop ports (DPs) are obtained, compared to their 1st-order counterpart, the ER at through ports (TPs) are deteriorated much. The residual optical power at TRs increases the CT to DPs. This phenomenon is alleviated in the 10-μm-radius 3rd-order MRR filters, as shown in Figure 2(g), but the resonance shift possibility caused by fabrication errors increases with more rings so that it needs microheaters to control. From the footprint perspective, fewer rings are costive. So in the large MRR-based photonic network, it suggests to use single MRR filters as much as possible. Figure 2(h) shows the measured ER at TPs and DPs and the insertion loss of DPs varies with

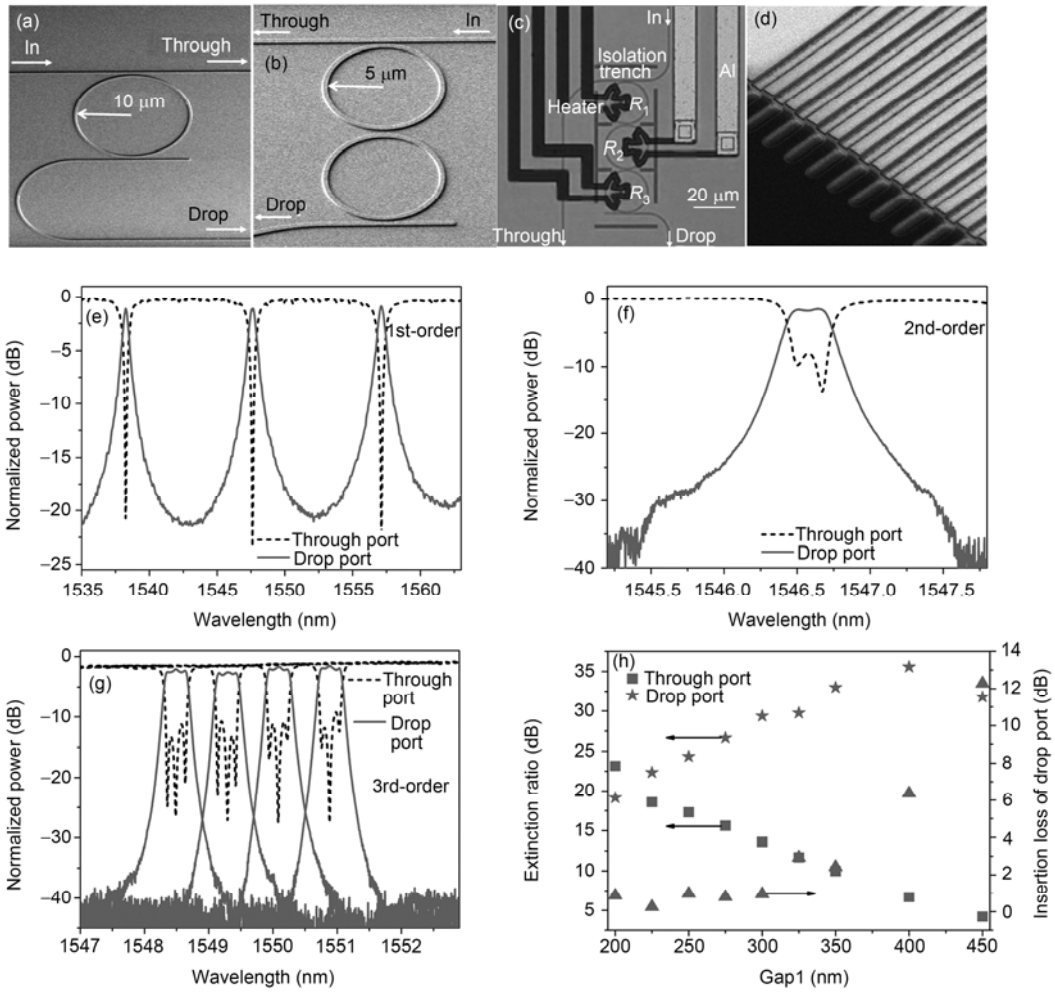


**Figure 2** Scanning electronic micrograph (SEM) of (a) 10-μm-radius 1st-order and (b) 5-μm-radius 2nd-order MRR filters; (c) micrograph of the 10-μm-radius 3rd-order MRR filter; (d) SEM of the grating coupler; (e),(f) response spectra of MRR filters in (a) and(b); (g) response spectra of the 3rd-order MRR filter in (c) tuned in 0.8-nm increments; (h) ER and insertion loss at drop port of the 10-μm radius 1st-order-MRR filter [61, 62].

Gap1. We can find that when Gap1 is less than 300 nm, the ER at TPs and DPs and the insertion loss of DPs are all in the acceptable range. This information is useful for knitting a MRR-based photonic network.

### 3.2 Si MRR-based wavelength-selective non-blocking optical routers

In 2008, Sherwood-Droz et al. [63] demonstrated the space-switched 4×4 hitless optical routers by utilizing thermal tuning MRR switches. The dynamic TO tuning of MRRs needs power consumption and additional switching time (the TO tuning speed is very low, in the order of 10 kHz). Considering the pros and cons, we designed the Si MRR-based wavelength-selective non-blocking optical routers for our previously proposed PNoC [64, 65], rather than that for CSPIN. However, by changing the MRR location and numbers, the MRR-based wavelength-selective non-blocking optical routers can be converted to the optical crossbar switches [18], which constitute the OSU in our proposed CSPIN router.

Figures 3(a) and 3(b) show the schematic configuration and micrograph of a demonstrated Si MRR-based wavelength-selective (WS) 4 × 4 non-blocking optical router [66]. The four ports are labeled as North (N), South (S), East (E), and West (W). Each port includes input and output channels, e.g. $N$ port has the input channel $N_i$ and output channel $N_o$. Two groups of MRRs are designed with the radii of 10 and 10.01 μm, respectively, to obtain resonant wavelengths of $\lambda_1$ and $\lambda_3$ that have the 100-GHz channel spacing. When signals with wavelength of $\lambda_1$, $\lambda_2$, and $\lambda_3$ are injected into one of the input ports, they will be routed to three different output ports according to their resonant conditions (no U-turn is allowed). The router has 12 possible I/O routing paths and presents 13 non-blocking operating states, including four broadcasting states. The fabrication process is the same with the 3rd-order MRR filter mentioned above. The measured optical response spectra of 12 paths of the

router are shown in Figure 3(c). The worst ER and CT of the device are 21.05 and −21.56 dB. In the experiment, TiN heaters consume power of 49.95 mW for thermal tuning to compensate the resonances shift of MRRs caused by fabrication errors.

Table 1 gives the comparison of the performances of 4×4 silicon-based optical routers/switches mentioned above. It is clear to see that small element dimension is the common advantage of the MRR-based routers/switches compared with the MZI-based routers. But the shortcoming is that they usually have the narrow optical bandwidth, which limits them to realize the WDM routing. The MRR-based devices demonstrated in refs. [66–68] adopt the passive wavelength-selective operating principle. Among them, our device exhibits much lower CT but at the sacrifice of more power consumption. It is due to that the devices demonstrated in refs. [67, 68] are true passive without power consumption. However, in practice, the fabrication errors lead the MRR's resonant wavelengths shift and results in the extremely large CT of these devices (as seen in Table 1), which will deteriorate the quality of signal transmission, even cause the bit error. For the sake of reducing the CT, it is worth to use heaters to compensate the fabrication errors though they expend power. And by optimizing the device structure, e.g., using MRRs with undercuts, the power consumption will decrease greatly. Such approaches can make a trade-off between the CT and power consumption. We also designed a Si MRR-based wavelength-selective 4×4 optical crossbar switch that is similar to those demonstrated by Kazmierczak et al. and Zhou et al. [67, 68], for the purpose of the OSU realization. Now the chip is under manufacturing.

### 3.3 MZI-based multiport switches

Another approach to implement the OSU is to use the MZI-based multiport switches, which have the advantages of characteristic stability, large spectral bandwidth and fabrication tolerance [69–76]. The most remarkable work among these was done by Yang et al. [77]. They demonstrated a 4×4 non-blocking switch by using the EO switching MZIs in 2010. The device supports a wide optical spectral bandwidth of 7 nm with worst-case CT lower than −9 dB. High-speed 40 Gbps data transmission experiments verify optical data integrity for all input-output channels. We started the research of the MZI-based optical switches in 2007 supported by the National Natural Science Foundation of China. This part summarizes some of the MZI-based switches we demonstrated by CMOS process.

#### *3.3.1 2×2 EO switch*

The 2×2 EO switch is the basic element in the optical router and the PNoC. The phase modulation manner of Si EO switches is based on the FCD effect. However, the free carrier absorption (FCA) effect coexisting with FCD effect in Si is a detrimental behavior that can influence the CT and ER of interference-based optical devices, which caused the CT of the reported EO switches seldom below –20 dB. In

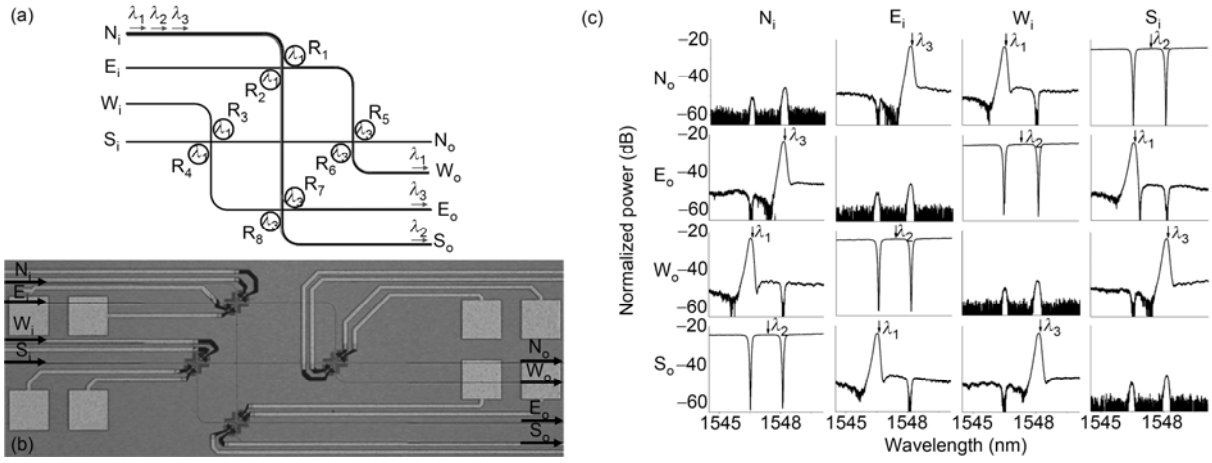


**Figure 3** (a) Schematic structure; (b) micrograph and (c) optical response spectra of 12 paths of the 4×4 non blocking optical router [66].

**Table 1** Performance comparison with 4×4 silicon-based optical routers/switches

| Type | Element dimension (μm) | Average power consumption (mW) | Optical bandwidth (nm) | Worst ER (dB) | Worst CT (dB) | Year | Reference |
|---|---|---|---|---|---|---|---|
| MRR & TO | 10 | 6.5 | 0.308 | 20 | not given | 2008 | [63] |
| MRR & WS | ~2 | none | not given | not given | –5.18 | 2009 | [67] |
| MRR & WS | ~10 | none | 0.55 | not given | –2.87 | 2009 | [68] |
| MZI & EO | >200 | 13.3 | 7 | 25 | –9 | 2010 | [77] |
| MRR & WS | ~10 | 12.5 | 0.2 | 21.05 | –21.56 | 2011 | our work [66] |

order to reduce the CT, we improved the traditional structure and demonstrated a 2×2 MZI-based EO switch [78]. The schematic structure is shown in Figure 4(a), composed of a 2×2 EO switch integrated with a variable optical attenuator (VOA) that is used to remove the undesired optical power. Rib waveguides with a cross section of 450 nm × 220 nm and a 60-nm-thick slab are adopted. The device design is carried out by the 3D beam propagation method. The fabrication process is similar to the MRRs mentioned in Section 3.1, expecting the ion implantation to form the p-i-n diode. Figure 4(b) shows the micrograph of the 2×2 MMI in the fabricated device. The measured static characteristics of the 2×2 optical switches are shown in Figures 4(c) and 4(d). As seen from the figures, in the "OFF" state, the VOA improves the CT of −10 dB, at the sacrifice of 24.4 mW additional power consumption.

The main performance parameters of the recently demonstrated 2×2 silicon-based EO switches by other research groups are listed in Table 2 to make a comparison with that demonstrated by us. As can be seen, the CT of our switch is in the first rank. Meanwhile, the optical bandwidth and switching time are at the middle level. The less-than- ideal performance of our device is that the power consumption is large in contrast to others. This attributes to the additional power consumption on the VOA. Increasing the doping concentration of the p-i-n diode or decreasing the cross section of the Si waveguide is helpful to reducing the power consumption. These will be considered in device design in future.

### *3.3.2 3×3 TO switch*

In multi-way optical switches, we suffer the problem of accurately controlling the phase shift magnitudes of many independent phase shifters, which results in a complex control system as well as additional cost and footprint. Moreover, the number of the employed phase shifters will dramatically increase and the problem will get worse when we construct a large scale photonics network or switch matrix. To solve these problems, we demonstrated a highly-integrated 3×3 MZI-based TO switch using a single combined phase shifter. The structure can be expanded to $N\times N$ without extra phase shifters [79]. Figures 5(a) and 5(b) show the schematic configuration and micrograph of the 3×3 MZI-based TO switch. The input light routed to which output port depends on the combined phase modulation group (denoted by $\varphi_c$) [80]. In the 3×3 MZI-based TO switch, arm 1 is set as the reference arm and $\varphi_c$ is equal to (0, 4π/3, 2π/3). So the length of the TiN heater of arm 2, as shown in

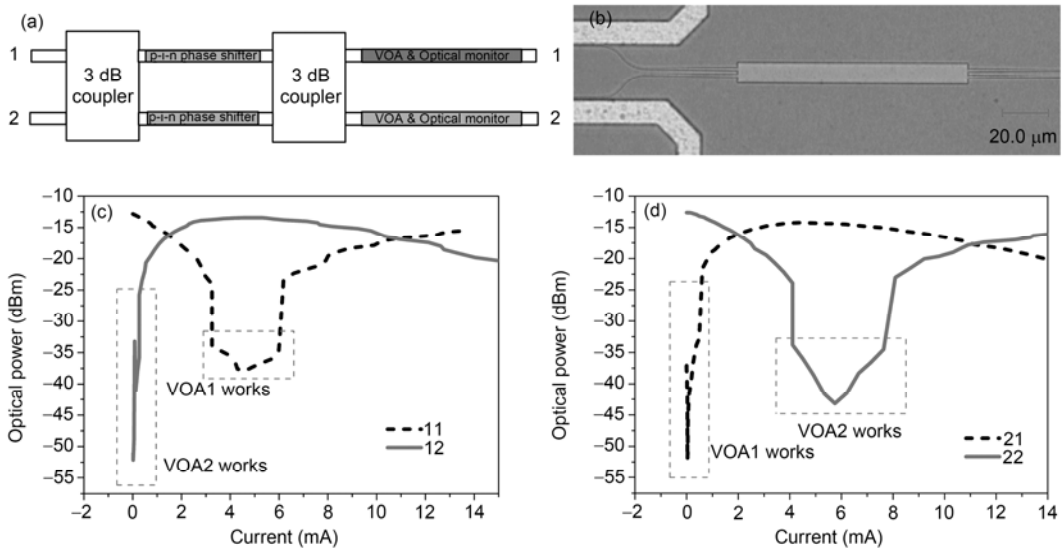


**Figure 4** (a) Schematic structure of the 2×2 EO switch integrated with VOA; (b) micrograph of the 2×2 MMI. Static characteristics of the 2×2 EO switch integrated with VOA when light is launched into (c) port1 and (d) port2 [78].

**Table 2** Performance comparison with 2×2 silicon-based EO switches

| Electrical/ optical structure | Element dimension (μm) | Power consumption (mW) | Optical bandwidth (nm) | Worst CT (dB) | Switching time (ns) | Year | Reference |
|---|---|---|---|---|---|---|---|
| p-i-n/MZI | 1000 | 9.4 | not given | –28 | 6.8 | 2009 | [69] |
| p-i-n/MZI | 200 | 3 | 110 | –17 | <4 | 2009 | [70] |
| p-i-n/MRR | 40 | 17.4 | 0.48 | not given | 7 | 2009 | [71] |
| p-i-n/MRR | 20 | 5.3 | 0.14 | –23 | <0.4 | 2010 | [72] |
| p-i-n/MZI | 4000 | 0.6 | 60 | –17 | 6 | 2010 | [73] |
| p-i-n/MZI | 2600 | 26.9 | 28 | –24.5 | 5.1 | 2011 | our work [78] |

Figure 5(a), is twice that of arm 3. The dimension of the MMI is 9 μm × 202.4 μm. The waveguide's cross section and device fabrication process are completely the same with the 3rd-order TO-tuning MRR filters discussed in Section 3.1. Table 3 depicts the operating manner of the proposed optical switch. Based on it we measured the static and dynamic characteristics of the fabricated 3×3 TO switch. The results, as shown in Figures 5(c)–5(e), illustrate that the multi-way switching function is realized with average CT of −11.1 dB and max switching power of 97.5 mW. The spectral bandwidth of the switch is characterized by launching light to input port2 and switching to output port3. The bandwidth of the status 2–3 is 5 nm (1555.5–1560.5 nm), with wavelength-dependent loss lower than 0.4 dB. The switching time was less than 14.2 μs, which can be improved to sub-μs by introducing the drive circuit [81], or improved to a few nanoseconds by employing the EO polymer-clad Si slot phase shifter [82].

### 3.3.3 *Four-port EO routing switch*

The reported routing switches are mostly based on MRRs, here we introduce a 4-port optical routing switch. As shown

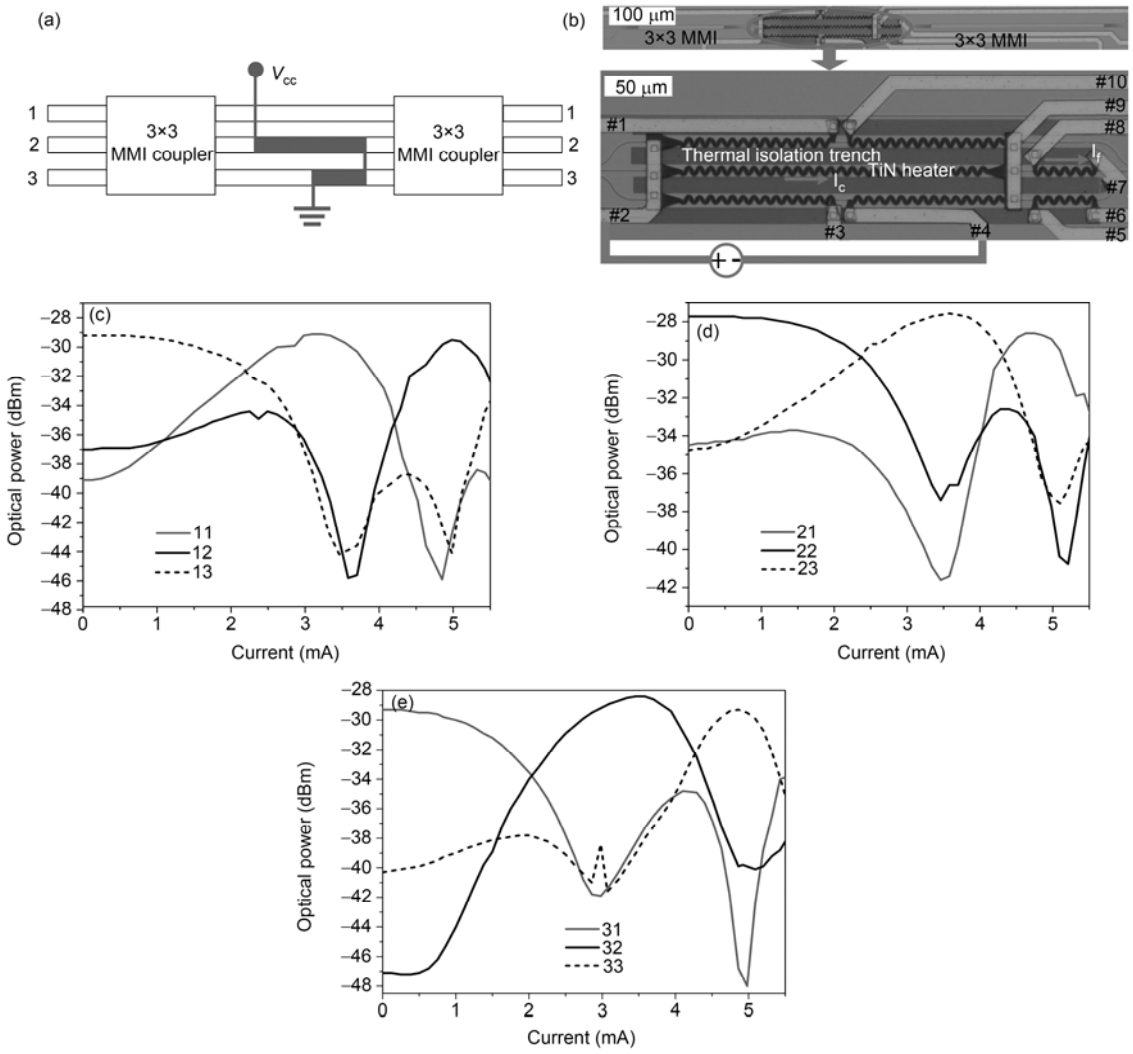


**Figure 5** (a) Schematic structure and (b) the microscope image of the 3×3 TO switch. Static characteristics of the 3×3 TO switch when light is launched into (c) port1, (d) port2 and (e) port3 [79].

**Table 3** Operating manner of the proposed 3×3 TO switch [79]

| $\varphi_c$=[0, 4π/3, 2π/3] | Output port | | |
|---|---|---|---|
| | $\varphi_c$×0 | $\varphi_c$×1 | $\varphi_c$×2 |
| Port1 excited | Port3 | Port1 | Port2 |
| Port2 excited | Port2 | Port3 | Port1 |
| Port3 excited | Port1 | Port2 | Port3 |

in Figure 6(a), it is constructed by four 1×3 MZI-based EO switches and one crossing waveguide [83]. The switch possesses two operating modes: the routing mode and broadcasting mode. As depicted in Table 4, in the routing mode, optical path is built between any two ports. While in the broadcasting mode, optical signals are broadcasted to the other three ports. The 1×3 MZI-based EO switches have been successfully demonstrated by us using both the 0.8- and 0.13-μm CMOS technology [83–85]. We draw on the experience of it to design the 1×3 MZI-based EO switches here used to build the 4-port EO routing switch. The waveguide's cross section and device fabrication process are identical with the 2×2 EO switch mentioned in Section 3.3.1. Figure 6(b) shows the micrograph of the fabricated device. Because the chip has not been packaged, we did not measure the response spectra of the output port which is located in the same side with the input port. A part of measurement results is shown in Figures 6(c) and 6(d). The router has a broad operating band (8 nm) and low CT (<−10 dB). Low power consumption (<20 mw) and fast response time (< 6.2 ns) are achieved by using the p-i-n diode-driving phase shifters.

## 4 Conclusions

In summary, this paper reviews the recent developments in Si photonics for OI (including PNoC and optic-link enabling components) and presents our approach to realize the PNoC by utilizing the Si photonic technology. We proposed a novel CSPIN to connect multi cores and made efforts on Si devices to implement the key component of the proposed CSPIN: the CSPIN router. The demonstrated Si MRR-based optical add-drop filters, wavelength-selective non-blocking optical router, and MZI-based multiport switches are summarized as the work foundation to design and fabricate the

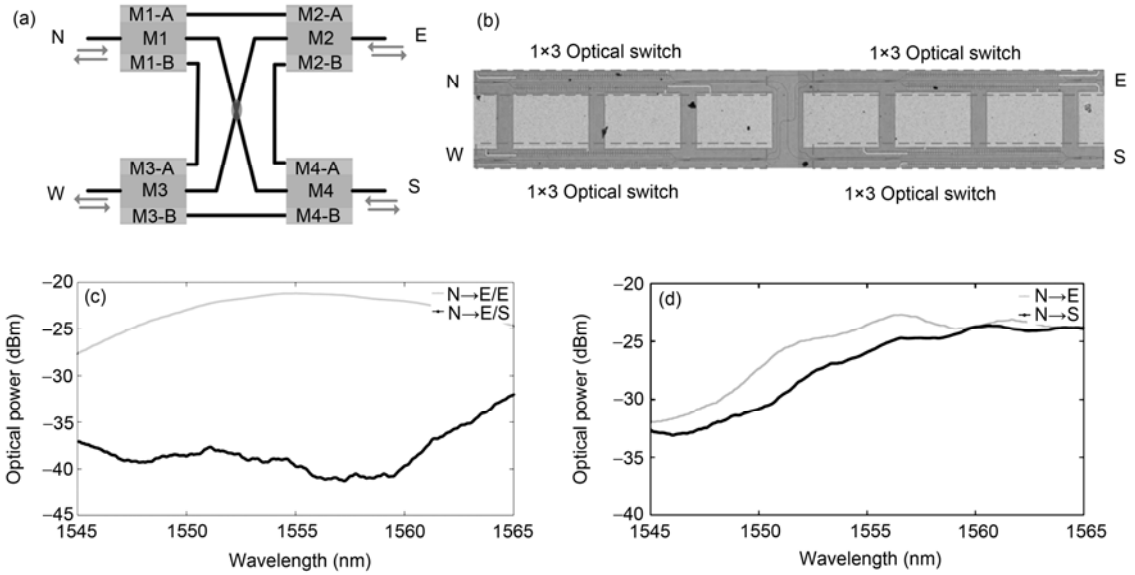


**Figure 6** (a) Schematic structure; (b) microscope image; (c) routing mode: E→N; and (d) broadcasting mode: N→E and S of the 4-port routing switch [83].

**Table 4** States of the 4-port optical routing switch [83]

| | | | Linked path | Phase shifters used |
|---|---|---|---|---|
| Switching state | routing mode | 1 | N ←→E | M1-A & M2-A |
| | | | W←→S | M3-B & M4-B |
| | | 2 | N ←→S | M1-A, B & M4-A, B |
| | | | W←→E | M2-A, B & M3-A, B |
| | | 3 | N ←→W | M1-B & M3-A |
| | | | E ←→S | M2-B & M4-A |
| | broadcasting mode | 4 | N→E/W/S | M2-A/M3-A/M4-A&B |
| | | 5 | W→N/E/S | M1-B/M2-A, B/M4-B |
| | | 6 | E→N/W/S | M1-A/M3-A, B/M4-A |
| | | 7 | S→N/W/E | M1-A, B/M3-A/M2-A |

OSU. The EO-tuning MRR and PD-based RU, TU and FU are under fabricating. Though there will be a set of serious challenges to integrate these components together to operate coordinately, the potential reward of the OI makes it worth to do.

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