Circuit-Switched On-Chip Photonic Interconnection Network

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ABSTRACT: In this paper, we propose a novel circuit-switched on-chip photonic interconnection network (CSPIN) architecture. Different from existing circuit-switched photonic networks, CSPIN eliminates the electronic control layer but employs optical signaling to control the circuit switching functions. To implement CSPIN, the CSPIN router is proposed which uses electro-optical tuned micro-ring resonators. The analysis based on the synthesis result of the CSPIN router shows that significant savings in power and path-setup latency are achieved by the proposed CSPIN architecture.
Keywords: Circuit-Switched Network; Photonic Network-on-Chip; Micro-Ring Resonator

1. Introduction

Silicon photonic interconnects have been long considered as a promising candidate to overcome the limitations of electrical on-chip interconnects. In recent several years, a number of on-chip photonic interconnection network architectures have been proposed, which can be classified into non-blocking networks, circuit-switched networks, and packet-switched networks. Circuit-switched photonic network architectures take advantage of the optical spectrum by establishing a high-bandwidth light path dedicated for data transmission [1]. Existing circuit-switched on-chip photonic networks include the hybrid folded-torus photonic-electronic network [2], the hybrid mesh network [3], the fat-tree based optical network [4], and the memory access network etc [2]. In most of these architectures, an additional electronic control network is used to setup, release, and control the optical circuits (aka light paths). However, separation of the optical layer and the electronic control layer may impose significant latency overhead of circuit-setup and dramatically increase the power consumption and integration complexity. As studied in [2], the electronic control network attributes a large portion of the total power consumption.

In this paper, we propose the circuit-switched photonic interconnection network (CSPIN) aiming to reduce the power consumption and latency of the signaling process. Different from existing circuit-switched networks, CSPIN eliminates the electronic control layer but employs optical signaling to control the circuit switching functions, including the setup, confirmation and release of the optical circuits. An innovative optical router design is proposed to implement CSPIN. The analysis based on the synthesis result of the CSPIN router shows that significant power saving is achieved by the proposed CSPIN architecture.

2. CSPIN Architecture

2.1 Overview of CSPIN

Fig. 1 shows the logic view of a CSPIN which consists of two layers: the computation layer and the photonic layer. The computation layer is composed of the processing cores organized in clusters and local communication facilities. The photonic layer consists of the photonic interconnection network built with waveguides and optical routers. The CSPIN in Fig. 1(b) is composed of 64 nodes organized in 16 clusters which are interconnected by a 4×4 optical mesh. Inside a cluster, the four nodes are connected by an electronic router (ER), which is connected to an optical router (OR). Each OR has four optical channels, each connected to the adjacent four ORs in the network.

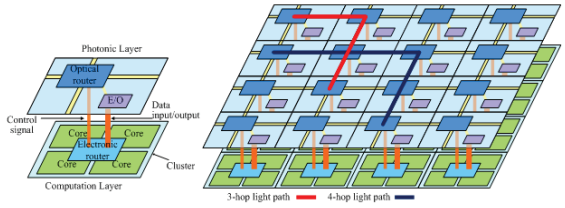

Fig. 1. (a) Single node structure in CSPIN; (b) CSPIN with 64 cores.

In CSPIN, intra-cluster communication is handled by the ER inside each cluster and inter-cluster communication is performed by the optical network. Before any two clusters (referred as nodes in the optical network) communicate, a dedicated light path from the source node to the destination node will be built first. The light path is composed of a sequence of photonic channels. A 3-hop light path and a 4-hop one are shown in Fig. 1(b). The light path will be released after data transfer is finished. The novelty of CSPIN lies in that all circuit switching functions are realized by optical signals.

2.2 Circuit Switching Functions

In CSPIN, communication via circuit switching includes four phases: Circuit Setup, Circuit Confirmation, Data Transmission, and Circuit Release. In the circuit setup phase, the source node will send the circuit setup slices to each intermediate node to reserve a channel. In the circuit confirmation phase, the source node will send circuit confirmation slices to verify if the path is successfully built. Next, in the data transmission phase, the source node will send the data to the destination node. After the data is successfully received by the destination node, the source node will send circuit release slices to the destination node and the intermediate nodes to release the circuit. Note that the proposed circuit switching scheme can be applied to any 2D and 3D direct network topologies.

Fig. 2 shows the optical data frame comprised of four fields corresponding to the above four phases. Each frame is generated by the source node and under the fully control and monitoring of the source node. All other nodes on the light path receive the optical signals and control the circuits to setup/reject/release the optical circuit. No optical signal will be generated at each intermediate node. By this way, the control logic and the number of EO interfaces needed at each intermediate node are minimized.

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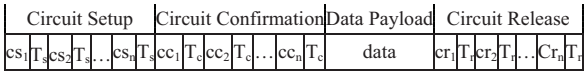


Fig. 2. Data frame structure in CSPIN.

Circuit Setup (CS) Field: Assume there are n hopes between the source and destination nodes, the CR field thus contains n header slices cs_1, ⋯, cs_n, each used for requesting an output channel at an intermediate node, respectively. Each header slice contains the routing info (such as the output channel no/destination address). Between two adjacent header slices an idle time slice is inserted to accommodate the channel reservation delay at each intermediate node. Once receiving the corresponding header slice of the CS field, each intermediate node will check if the output channel is available and reserve the output channel or reject the circuit setup request. When the destination node reserves the channel, a light path is setup from the source node to the destination node.

Circuit Confirmation (CC) Field: Similar to the CS field, the CC field is composed of a set of confirmation slices interleaved with idle time slices. In case that an intermediate node or the destination node has no channel to allocate, the CC field will be fed back from the node to the downstream intermediate nodes and the source node.

Data Payload (DP) Field: The DP field consists of the data payload generated from the source node. If the light path is successfully setup (i.e., no confirmation slice is fed back), the source node will transmit the DP field to the destination node through the light path.

Circuit Release (CR) Field: CR field is with similar format to the CC field. When the destination node receives the first slice of the CR field (i.e., DP field is received), it will feed back the remaining slices to all downstream nodes. At each intermediate node, after receiving the corresponding slice, it will release the reserved channel.

2.3 Routing Algorithms in CSPIN

Two types of routing algorithms are considered in CSPIN: predetermined routing and adaptive routing. According to the routing algorithm selected, in the CR phase, the CR field content and the routing function performed at each node will be different. Note that CSPIN inherently avoids deadlocks with either routing algorithm.

In *predetermined routing*, the route is determined by the source node. The output channel requested at each node is specified in the corresponding header slice. Each intermediate node simply checks the availability of requested channel to setup the circuit. The major benefit of this routing algorithm is its simplicity which minimizes the setup time experienced at each node.

In order to achieve better throughput and load balance, *adaptive minimal routing* can be used. In this case each CS slice need carry the destination address and related info. The tradeoff is the increased complexity of the control circuit and longer setup time at each node.

3. CSPIN Router Structure

Fig. 3 shows the conceptual block diagram of the CSPIN router, which consists of Detecting Units (DU), Feedback Units (FU), Reversing Unit (RU), Optical Switching Unit (OSU), Transceiver Units (TU), and Routing Control Unit (RCU). Note that each input channel is associated with a DU and a RU.

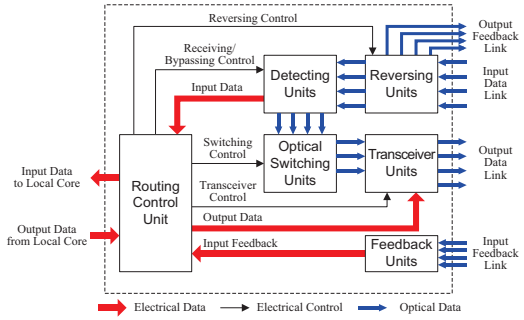
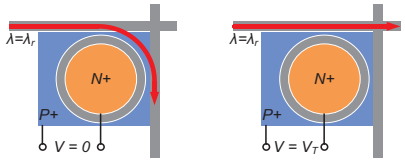


Fig. 3. Structure of a 4-channel CSPIN router.

Electro-Optical (EO)-tuned MRRs are integrated in DU, RU, TU and OSU, as the basic switching devices due to the superiority of EO tuning in fast on/off time, low power consumption and small footprint [5]. Fig. 4 shows the operation of an EO-tuned MRR-based optical switch. All MRRs have the same size (corresponding to the input wavelength) and can switch between two working modes: *resonating* and *bypassing* (i.e., on and off in Fig. 4) by removing/injecting the tuning current applied on the MRR. The rationale of this setting is to reduce the absorption of optics by electrons when the tuning current is injected.



(a) Without tuning current. (b) With tuning current.

Fig. 4. EO-tuned MRR.

As shown in Fig. 3, each CSPIN router has n (in this example n = 4) optical channels which are connected its neighbor CSPIN routers. Each optical channel is comprised of four links: input/output links and input/output feedback links. Input/output feedback links receive/feedback signals from/to other routers during each communication. The two electronic channels (data/control) connect the CSPIN router to the local electronic router. A single optical wavelength is used at all CSPIN routers.

Detecting Unit: The conceptual block diagram of the Detecting Unit of a channel is shown in Fig. 5(a). The DU uses one MRR to extract light from input channel when it is working on receiving mode. When the MRR is tuned (current injected to the PIN) it will be blind to the channel. Two photodetectors are used to receive the signals from the input link and feedback link, respectively.

In the circuit release phase, the optical receiver on the incoming feedback link will receive the corresponding slice in the circuit release field. The converted electronic signals will be passed to the RCU which will release the reserved channel and set the data receiving MRR back to the receiving mode.

Reversing Unit (RU): The conceptual block diagram of the Reversing Unit of a channel is shown in **Error! Reference source not found.**5(b). The RU works like a mirror to reflect all optical signals from the input link to the output feedback link. One MRR is used to reverse the signals. Normally the MRR is tuned to the bypassing mode so that the optical signals are passed through the RU straightly. When the current is removed the MRR will be switched to the reversing mode to reverse the input optical as the feedback to its original node.

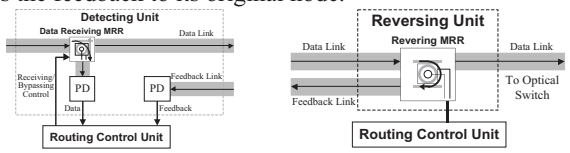


Fig. 5. (a) Detecting unit and (b) Reversing Unit.

Optical Switching Unit (OSU): The OSU is an $n \times n$ optical crossbar switch. The RCU controls the tuning of MRRs to set the route from an input link to an output link. At any time, only one output can be assigned to one input, and vice versa.

Transceiver Unit (TU): An E/O tunable MRR is assigned at each output data link to inject optical signals. The MRR works as a modulator to add outgoing data on the optical carrier from the laser.

Routing Control Unit (RCU): The RCU is the heart of the router which performs the functions of routing and controlling all other units. The RCU structure is shown in Fig. 6. In the circuit setup phase, once receiving the routing info, the RCU will compute the output channel. If the output channel is available, it will reserve both input and output channels by setting all related MRRs in the OSU and setting the DU to bypass the signals; otherwise, it will reject the circuit setup request by setting the RU to feed back the signals. In the circuit release phase, once receiving the circuit release slice, it will release the reserved channels by setting the OSU and setting the RU to feed back the signals.

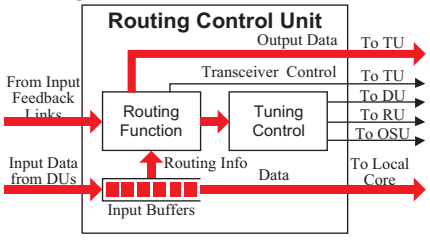


Fig. 6. Routing Control Unit

4. Power Consumption and Transmission Latency

To evaluate the proposed CSPIN, we first implement the RCU of a 4-channel CSPIN router and synthesize it under 65nm technology. For comparison, the same performance metrics of a matching circuit-switched electronic network (running at 625MHz with 16-bit flit size) are derived based on the results obtained from Orion 2.0 [6]. Tab. 2 and Tab. 3 show the overall power consumption and signaling latency of CSPIN (with the photonic device parameters given in Tab. 1) and the electronic network with different hop-count paths given the data payload size of 8KB, respectively. CSPIN achieves significant savings (over 90% in power and 65% in path-setup time) compared with the electronic control network.

Table 1. CSPIN Router Photonic Device Parameters

Channel Bandwidth	10Gbps
Frequency	Optical: 10GHz, Electrical: 2.5GHz
Serializer	4:1, power: 10mW [7]
Deserializer	1:4, power: 10mW [7]
MRR EO Tuning	On: 20fJ/bit, Off: 5fJ/bit [8]
Modulator & Detector	2pJ/bit [2]

Table 2. Power Consumption Comparison

Power Consumption Per Frame Transmission (J)		Hops			
		4	6	10	14
CSPIN	Signaling	0.11	0.17	0.28	0.39
	Data Transmission	304.95	308.95	316.95	324.94
Electronic Network	Signaling	1.54	2.78	6.28	11.14
	Data Transmission	725.03	874.06	1172.13	1470.20

Table 3. Signaling Latency Comparison

Hops	4	6	10	14
CSPIN	7.20	10.8	18	25.2
Electronic network	28.8	38.4	57.6	76.8

5. Conclusion

In this paper, the CSPIN architecture is proposed and analyzed. In CSPIN, the circuit switching functions are controlled by optical signals. As confirmed by the analysis, CSPIN significantly reduces the power consumption and latency of the circuit-setup phase. In addition, it can help reduce the integration complexity of the on-chip interconnection network.

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