Performance Study of Packet Switching Multistage Interconnection Networks

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ABSTRACT

This paper provides a performance study of multistage interconnection networks in packet switching environment. In comparison to earlier work, the model is more extensive – it includes several parameters such as *multiple-packet messages, variable buffer size,* and *wait delay* at a source. The model is also uniformly applied to several representative networks and thus provides a basis for fair comparison as well as selection of optimal values for parameters. The complexity of the model required use of simulation. However, a partial analytical model is provided to measure the congestion in a network.

I. INTRODUCTION

interconnection Multistage networks (MINs) are used in multiprocessing systems to provide cost-effective, high-bandwidth communication between processors and/or memory modules. A MIN normally connects N inputs (sources) to N outputs (destinations) and is referred to as an $N \times N$ MIN. The parameter N is called the size of the network. There are several different multistage interconnection networks proposed and studied in the literature, including Delta network [1], Binary n-cube network [2], Omega network [3], Gamma network [4], Kappa network [5], Multipath network with cross link [6], etc.

The networks can be unbuffered or buffered. In unbuffered networks with circuit switching, physical path must be established before the actual data transfer. Buffered networks with packet switching are more flexible in that packets are routed through the network without establishing a physical path.

Patel [1] analyzed the performance of unbuffered Delta networks in terms of the probability of acceptance (*PA*) of requests. Dias and Jump [7] extended Patel's analysis to buffered Delta networks. The measures of merit used for their analysis were the *average delay* of a packet and the *throughput* of a network. But their assumption that requests which are blocked in the course of routing are lost is unrealistic. Moreover, each message was assumed to consist of a single packet, which is not the case when message size is larger than the packet size. Davis and Siegel [8] extended the analysis of buffered Delta networks to include the use of multiple-packet messages, assuming a buffer size of four packets. Davis and Siegel's work is restricted to Delta networks. Recently, Yoon et al. [9] provided a study of buffered multipath MINs. However, their model does not consider multi-packet messages. Our research integrates the various aspects studied separately in [8], [9]. In addition, we introduce a refined metric called *wait delay* and the notion of *congestion-region* to provide a better understanding of the performance results.

We provide a comprehensive study to serve several purposes which include analyzing the performance impact of various parameters, optimal choices for network parameters, and the comparison of different networks. The results of our analysis provide a basis for better designs of interconnection networks by offering optimal choices for parameters like buffer size.

An analytical model is provided to measure the *wait delay* which is the time lost by a packet at the network source because of the unavailability of an empty buffer at the input stage of the network. The analytical model can determine the degree of traffic congestion inside a network without having to actually measure individual packet delays.

The simulation model and the operating environment are described in Section II. Section III describes the performance criteria and input parameters. Section IV explains the con-

Network	Control Strategy		
Delta	Destination Tag Algorithm		
Gamma	Unrestricted Routing		
Kappa	Fault-tolerant Destination Tag Algorithm		
Multipath network with cross link	H-route		

cept of congestion. The wait delay is described in detail in Section V. Section VI gives a brief description of the simulator. Simulation results are presented and discussed in Section VII and Section VIII provides the concluding remarks.

II. THE MODEL AND THE ENVIRONMENT

A packet switching multiprocessing system can be organized as a tightly coupled system in which the network sources are processors and the network destinations are memory modules, or as a loosely coupled system in which the sources and the destinations are the same processors, each with its own local memory. Our analysis is applicable to both types of system organizations.

In a packet switching system, a message is divided into fixed sized packets which are normally of the same size as the network's path width. We assume that bounded buffers (fixed sized, first-in first-out queues) are placed in front of all input ports of each switching element (SE). The size of a buffer refers to the maximum number of packets that it can hold. A packet may experience *blocking* either because of a network conflict, i.e., other packets compete for the same output link of an SE or because of a full buffer at the next stage.

We analyze and compare four representative buffered MINs in Table 1. The networks are illustrated in Fig.1. The details of these networks can be found in [1], [5], [6], [10].

A timing parameter has to be selected to model the operation of a packet switching network. We will use the timing parameter packet cycle time (τ) as introduced by Davis and Siegel [8]. It is defined as the time required by a packet to pass from the head of an SE's input buffer to the input buffer of an SE at the next stage. The packet cycle time will be the unit of time and we will often refer to it as the *network cycle*. The *packet offset time* (α) represents the time interval between the generation of successive packets. This time interval is the amount of time for a network source to form a com-



Fig. 1. Four representative MINs

plete packet and place it in the *source buffer*. A source buffer of size one is assumed to be associated with each network source. A representative packet switching network, an 8×8 Delta network, is shown in Fig.1 (a). The packet offset is assumed to be a multiple of a packet cycle time as in [8].

Each network source is in one of the three possible states: *idle*, *busy* or *waiting*. When a packet is being generated, the source is in the busy state. If the packet offset time α is $k\tau$, then the source is busy during k network cycles. A source is in the waiting state if it is waiting for the source buffer to be available. When a source is neither busy nor waiting, it is said to be in the *idle state*. The *loading factor* λ is defined as the probability that a network source will generate a new message given that it is in the idle state. When a packet is blocked at the source because of a full buffer at the input stage, the source suspends generation of successive packets and enters the waiting state. A blocked packet is considered to be delayed at the source for a number of cycles until a buffer space at the input stage becomes available and the packet can be forwarded.

The networks are assumed to operate under the following conditions:

- 1. Packets submitted to the network input ports contain both the data to be transferred and the routing tag.
- 2. Each source generates messages and submits them to the network with a load-ing factor of one, i.e., the assumption of

maximum load for the worst case analysis.

- 3. Packets are removed from the network as soon as they reach a network output port, i.e., destinations are not a bottleneck of the network operation.
- 4. Each source generates messages independent of all other sources.
- 5. The messages are uniformly distributed across all the destinations.
- 6. The network operation is synchronous. The submission and the removal of packets to and from the network and the movement of packets from stage to stage occur at each network cycle.
- 7. The network is fault-free.
- 8. Any one of the conflicting requests is equally likely to be chosen for transfer in an SE. This implies that the conflict resolution policy is random and fair. The exception is the cross link network [6], where requests coming via the cross-link have higher priority in order to prevent infinite looping between the two SEs that form a loop.

III. PERFORMANCE CRITERIA AND VARIABLE PARAMETERS

To evaluate the performance of several packet switching MINs, we will use the following metrics. Let *T* be a relatively large time divided into *v* time intervals $(t_i, t_{i+1}]$. Let n(i)

denote the number of packets accepted by destinations during the time interval $(t_i, t_{i+1}]$.

1. Average throughput (*TP*) is the average number of packets that reach their destinations per network cycle. This metric is also referred to as the *bandwidth* of the network. Formally, *TP* can be expressed by

$$TP = \lim_{v \to \infty} \frac{\sum_{i=1}^{v} n(i)}{v}.$$

2. *Normalized throughput (NTP)* is the ratio of the average throughput *TP* to network size *N*.

$$NTP = \frac{TP}{N}.$$

3. Average packet delay (APD) is the average time a packet requires to pass through the network after it is generated by a network source. Formally, APD can be defined as

$$APD = \lim_{T \to \infty} \frac{\sum_{i=1}^{N(T)} T(i)}{N(T)}$$

where N(T) denotes the total number of packets accepted in time T and the T(i)represents the delay for the i^{th} packet. We consider $T(i) = t_w(i) + t_{tr}(i)$, where $t_w(i)$ (wait delay) denotes the time lost by the i^{th} packet waiting for the availability of an empty buffer at the input stage of the network. The second term $t_{tr}(i)$ denotes the time spent by the i^{th} packet after it is submitted to the network, i.e., the total time which includes the queueing delay plus the transmission delay at each stage of the network.

- 4. Normalized packet delay (NPD) is the ratio of the APD to the minimum packet delay which is simply the transmission time. The minimum packet delay of a *k*-stage network is just $k\tau$, where τ is the network cycle.
- 5. Average message delay (AMD) is the average time that elapses between the generation of the first packet and the delivery of the last packet of a message.
- Normalized message Delay (NMD) is the AMD normalized by the minimum message delay. The minimum message delay of an *m*-packet message is [k + (m-1)]τ for a network with k stages.

The following parameters affect the delay and the throughput of packet switching networks.

- *buffer size* (β): maximum number of packets that an input buffer of an SE can hold. The range for β is assumed to be 1, ..., 8.
- *message size (m):* the number of packets comprising a message. The range is assumed to be 1, 2, 4, 8, 16.
- *packet offset* (α): time required to generate a packet. The range is assumed to be 1, ..., 15.

loading factor (λ): probability of generation of a new message given that a source is in the idle state.

In addition, for the the Gamma and the Kappa networks, we also study the effect of multiplexer SEs at the output stage.

IV. THE CONGESTION REGION AND THE CONGESTION THRESHOLD

To facilitate the understanding of the behavior of buffered networks, we introduce the concept of congestion which can also be found in [11]. Networks with bounded buffers may function in one of two operating regions. One is congestion region where sources experience non-zero wait delay t_w . The other is noncongestion region where $t_w = 0$. The boundary between the two regions is called the congestion threshold. The operating region of the network depends on the buffer size and the packet offset time. Thus we can represent the congestion threshold as the pair CTR(x, y) where x is a packet offset and y is a buffer size and the combination results in a congestion threshold. Our results show that for a given buffer size, it is always possible to operate below the congestion threshold by increasing the packet offset time. But it may not be possible to operate below the congestion threshold by increasing buffer size when the packet offset is one. A network will be called *heavily loaded*, if the packet offset time is one.

V. MATHEMATICAL MODEL FOR THE WAIT DELAY

In this section, we present an analytical model for the wait delay. As defined in Section II, let λ be the probability that a network source generates a *new message* in a given network cycle, given that the source is in the idle state. A packet switching MIN with bounded buffers can be thought of as a queueing system as shown in Fig. 2. The blocking probability of a request depends on the loading factor λ , message size *m* and packet offset α . To find the wait delay t_w per packet, we define λ_p as the probability that a network source generates a *packet* in a given network cycle. Since the average time between message generations is given by

$$\alpha m + \sum_{i=1}^{\infty} i(1-\lambda)^i \lambda = \alpha m + \frac{1-\lambda}{\lambda}, \qquad (1)$$

we get,

$$\lambda_p = \frac{1}{\alpha m + \frac{1 - \lambda}{\lambda}} \cdot m$$
$$= \frac{\lambda m}{\alpha m \lambda + (1 - \lambda)}.$$
 (2)

$$\lambda_p = Load \rightarrow Queueing \\ \lambda_p \cdot P_B \leftarrow System \rightarrow \lambda_p \cdot (1 - P_B) = NPT$$

Fig. 2. A MIN thought as a blocking queue.

A packet generated by a source gets blocked if the buffer at the input stage is full. Let P_B denote the steady-state probability that a packet is blocked by the network. Then the packet submission rate becomes $N\lambda_p(1 - P_B)$ where N is the number of network sources. But this must be the same as the throughput *TP* as discussed in [11]. Thus

$$N \cdot \lambda_p \cdot (1 - P_B) = TP. \tag{3}$$

This reduces to

$$\lambda_p \cdot (1 - P_B) = NTP \tag{4}$$

where *NTP* is normalized throughput. *NTP* decreases with λ_p because of the reduced network loading. Since we assume maximum loading $\lambda = 1$, (2) implies λ_p is simply $1/\alpha$ and thus it is independent of the message size. Thus (4) becomes

$$\frac{1}{\alpha} \cdot (1 - P_B) = NTP. \tag{5}$$

As α increases, network load is reduced and there comes a point where P_B becomes zero and $NTP = 1/\alpha$. No network source experiences wait delay t_w beyond this value of α . This is the point that we defined as the *congestion threshold* for a given buffer size. For a given buffer size β , let α_{TR} denote the minimum value of packet offset (α) which results in $NTP = 1/\alpha$, then the congestion threshold is represented by $CTR(\alpha_{TR}, \beta)^1$. Since we are interested in the wait delay t_w , we will consider only the case where the network operates in the congestion region ($\alpha < \alpha_{TR}$). P_B can be obtained from (5),

$$P_B = 1 - \alpha \cdot NTP. \tag{6}$$

With no limit on the number of resubmissions of blocked packets, the average wait time for the successful transmission of a packet through the network is given by

$$t_w = \frac{1}{\lambda_p} \cdot \sum_{i=1}^{\infty} i(1 - P_B) P_B^i \tag{7}$$

$$=\frac{P_B}{1-P_B}\alpha.$$
 (8)

Each term in the summation of (7) indicates that a packet is rejected (blocked) *i* times before it is accepted by a network at the *i*th resubmission. The probability of being received without blocking on the *i*th resubmission is $(1 - P_B)$.

The wait delay can also be derived in another way. Since the steady-state ensures (5), P_B can still be obtained from (6). Then

$$t_w = \frac{packet \ cycles \ wasted \ because}{of \ blocking \ in \ time \ interval \ T} (9)$$

$$t_w = \frac{packet \ cycles \ wasted \ because}{total \ number \ of \ packets \ accepted}$$

$$t_w = \frac{packet \ cycles \ wasted \ because}{total \ number \ of \ packets \ accepted}$$

$$=\frac{T-T/\alpha(1-P_B)(\alpha)}{T/\alpha(1-P_B)}$$
(10)

$$=\frac{TP_B}{T/\alpha(1-P_B)}\tag{11}$$

$$=\frac{P_B}{1-P_B}\alpha.$$
 (12)

buffer size for a given packet offset α . Then the β_{TR} is the minimum buffer size which results in $t_w = 0$.

¹In contrast, a congestion threshold can be represented by $CTR(\alpha, \beta_{TR})$ if it is obtained by increasing a

Equation (12) is identical to (8).

In our simulation, the wait delay t_w and the congestion threshold α_{TR} will be extensively used. In the following section, we use our analytical model for the wait delay, once P_B is determined by simulation.

VI. SIMULATION

The performance evaluation of MINs is normally based on analytical model and simulation studies. Multiple-packet messages increase the complexity of the analytical model, making it difficult to get analytical solutions. The complexity of the analysis for multiplepacket messages results from dependencies among the packets comprising a message because they are sent to the same destination. We have developed a general purpose simulator to measure the delay and the throughput of a MIN. The results for networks of size 32 are reported in this paper.

Each simulation cycle corresponds to a network cycle. The number of simulation runs was adjusted so as to insure that the simulated network had reached a *steady-state* operating condition. Each simulation was run for 2000 cycles. Tests indicate that extending the run time had little effect on the simulation results. Lastly, each simulation was repeated five times and results were averaged in order to reduce the statistical variations. Detailed and comprehensive simulation results can be found in [12].

Validity of the analytical model for the wait

delay t_w was tested by comparing the analytical results with simulation which were found to be in close agreement (within 1 %). Where our results overlap the work done by others, our results agree with the earlier works [7], [8], [13].

VII. PERFORMANCE RESULTS

The performance results are discussed to show the effects of varying the different parameters, to find the optimal choices for parameters, and finally to compare different networks.

1. Packet Offset Effect

Representative plots for the normalized packet delay (NPD), the normalized message delay (NMD) and the wait delay t_w as a function of packet offset time α are shown in Figs. 3 and 4. As the packet offset increases the NPD decreases and approaches some minimum value. The minimum occurs after the congestion threshold $CTR(\alpha_{TR}, \beta)$ independent of the message size and the network type. As the packet offset increases, the load on the network diminishes and the traffic through the network decreases, thus reducing the delay t_w and time t_{tr} . The congestion threshold, α_{TR} , is indicated by the point where t_w becomes zero. The NMD initially decreases as the packet offset increases. However, the message delay increases after its minimum value at α_{TR} because the increased packet offset dominates the overall message delay, nullifying the effects of light network load.



Fig. 3. Variation of *NPD*, *NMD*, and t_w with different packet offset times – Delta network.



Fig. 4. Variation of *NPD*, *NMD* and t_w with different packet offset times – Kappa network.

For a fixed buffer size, the congestion thresholds $CTR(\alpha_{TR}, \beta)$ is reached with a lower packet offset for multipath MINs as compared to Delta network. Among the multipath MINs, the congestion threshold is reached with the lowest packet offset for the Kappa, followed by the Gamma, and the cross-link network, respectively. This order corresponds to the decreasing degree of multiple paths, with the Kappa network having the maximum number of multiple paths. The optimal packet offsets that minimize overall message delay for different combinations of message and buffer sizes are listed in Table 2.

A representative plot for the normalized throughput (*NTP*) versus packet offset time is shown in Fig. 5. The *NTP* is also seen to decrease with increased packet offset as the network load gets lighter. The *NTP* decreases more significantly when the operation of a network shifts from the congestion region to the non-congestion region. In the congestion region, increasing the packet offset time reduces the wait delay without significantly lowering the throughput.



Fig. 5. Variation of *NTP* for each network with different packet offset times

Networks	Message	Buffer Size				
Terworks	Size	1	2	4	8	
Delta	1 2 4	$5 \sim 10$ $5 \sim 10$ $5 \sim 10$	$\begin{array}{c} 2\sim5\\ 2\sim5\\ 2\sim5\\ 2\sim5\end{array}$	$2 \\ 2 \sim 5 \\ 2 \sim 5$	$\begin{array}{c}2\\2\\2\sim5\end{array}$	
	8 16	$5 \sim 10 \\ 5 \sim 10$	$2 \sim 5 \\ 2 \sim 5$	$2 \sim 5 \\ 2 \sim 5$	$2 \sim 5 \\ 2 \sim 5$	
Gamma	1 2 4 8 16	$2 \sim 5$ $2 \sim 5$ $2 \sim 5$ $2 \sim 5$ $2 \sim 5$ $2 \sim 5$	2 $2 \sim 5$ $2 \sim 5$ $2 \sim 5$ $2 \sim 5$	2 2 $2 \sim 5$ $2 \sim 5$	2 2 2 2 2	
Kappa	1 2 4 8 16	2 $2 \sim 5$ $2 \sim 5$ $2 \sim 5$ $2 \sim 5$	2 2 2 2 $2 \sim 5$	2 2 2 2 2	2 2 2 2 2	
Hybrid	1 2 4 8 16	$2 \sim 5$ $2 \sim 5$ $2 \sim 5$ $5 \sim 10$ $5 \sim 10$	2 $2 \sim 5$	2 $2 \sim 5$ $2 \sim 5$ $2 \sim 5$ $2 \sim 5$	2 2 $2 \sim 5$ $2 \sim 5$	

Table 2. Packet offset resulting in the congestion threshold $CTR(\alpha_{TR}, \beta)$.

2. Multiple Packet Effect

In a congestion region, given a packet offset and a buffer size, we observed that the average packet and average message delays (*APD* and *AMD*) increase with the message size. With larger message sizes, networks become congested due to the dependencies among constituent packets of a message. In the noncongestion region ($\alpha > \alpha_{TR}$), the *APD* is essentially the network's minimum delay. We found that the throughput (*TP*) is higher for smaller sized messages.

3. Buffer Size Effect

We analyzed the network performance as a function of the buffer size for both heavily loaded and modestly loaded networks. Fig. 6 shows the results for a heavily loaded Delta network, with message size of two. The APD as well as the AMD is seen to drop to a minimum value and then begin to increase as the buffer size increases. The turning point is found to occur with buffer size of two for all message sizes considered in the study. The t_{tr} part of the APD monotonically increases with buffer size as was found in [7]. The reason for the drop in the APD and the AMD at buffer size of two can be explained as follows. The fact that the wait delay t_w decreases with buffer size, as shown in Fig. 6, indicates that the network becomes less congested and the blocking due to full buffers is reduced. However, larger buffers introduce larger delays because packets fill the buffers and stay in the network longer, thereby increasing queueing delays as discussed in [7]. At some point the decrease in the wait delay t_w is offset by an increase in queueing delay. Since t_w does not decrease beyond the buffer size of two, increasing the buffer size beyond this point only increases the overall delay.



Fig. 6. Variation of *APD*, *APD* with t_{tr} only, *AMD* and t_w with different buffer sizes under the heavily loaded condition – Delta network.

For multipath MIN results, shown in Fig. 7, no turning point is observed for APD. This is because the effect of the wait delay t_w on the overall delay is not significant since the blocking probability in a multipath MIN is much smaller in comparison to Delta network. A multipath MIN has higher throughput than a comparable Delta network. However, higher throughput implies acceptance of a larger number of packets by the network which can potentially produce higher delays. This was generally observed to be true except in the cases of single-buffer Gamma and Kappa networks. The rate of increase in delay is the highest for the cross-link network, because the cross links in effect add more stages, thereby increasing the queueing delays of packets. Under heavy loads, as the buffer size increases, the NTP increases as shown in Fig. 8. But, the TP levels off as the buffer capacity increases. While

the *TP* increases and then levels off, the *APD* and the *AMD* become intolerable as the buffer size increases. Based on the tradeoffs between the delay and the throughput, we suggest in Table 3 the optimal buffer sizes for various networks.



Fig. 7. Variation of *APD* for multipath MINs with different buffer sizes under heavily loaded condition.



Fig. 8. Variation of *NTP* for each network under the heavily loaded condition.

With light or modest loads, delay for all networks can be characterized as follows. In the congestion region, increasing the buffer size increases delay. But, in the non-congestion region, as the buffer size increases *APD* and *AMD* levels off to constant values. Buffer sizes, β_{TR} , which result in the congestion threshold $CTR(\alpha, \beta_{TR})$ are listed for various networks in Table 3. The table entry marked "NA" means that the congestion threshold was not reached up to the buffer size of eight. We found that the congestion threshold $CTR(\alpha, \beta_{TR})$ is reached with smaller buffer sizes when the message size is smaller.

When the network is not heavily loaded, the *NTP* increases and then levels off as the buffer size increases. The knee corresponds to the point where the congestion threshold $CTR(\alpha, \beta_{TR})$ occurs.

4. Multiplexer SEs in the Kappa and the Gamma networks

In spite of more redundant paths in the Kappa network, it may have higher *APD* and *AMD* as compared to the Gamma network. This is observed when the networks are heavily loaded and the buffer size is larger than one. This apparent discrepancy occurs because of the multiplexer SEs at the output stage. The rate of packet transfers is one packet per each multiplexer SE for both the networks. Thus the output stage acts more of a bottleneck in the Kappa network than in the Gamma network. To investigate the effect of the output stage on the delay, we obtained the delay of

the Gamma and the Kappa networks, assuming that the SEs in the output stage can transfer all packets that are placed at the front of each input buffer in one network cycle. That is, a maximum of 3 packets can be passed to a destination at one time for the Gamma network, and maximum of 4 packets for the Kappa network. We call the resulting networks as the *enhanced Gamma* and the *enhanced Kappa* networks, respectively. The representative variations in *APD* are shown in Fig. 7 for both the networks. The delay in the enhanced Kappa network is greatly reduced compared to the enhanced Gamma network.

Table 3.	Buffer sizes resulting in the congestion thresh-
	old $CTR(\alpha, \beta_{TR})$.

Networks	Packet	Message Size				
11011101110	Offset	1	2	4	8	
Delta	2	4	8	NA	NA	
	5	2	2	2	2	
	10	1	1	1	1	
Gamma	2	2	2	4	8	
	5	1	1	1	1	
	10	1	1	1	1	
Kappa	2	1	1	2	2	
	5	1	1	1	1	
	10	1	1	1	1	
Hybrid	2	2	4	8	NA	
	5	1	1	1	2	
	10	1	1	1	1	

VIII. CONCLUSIONS

Our performance study of packet switching multistage interconnection networks is based on a comprehensive simulation model which includes several factors to represent the effects of the source and destination behavior. Many of the results obtained by earlier studies can be interpreted as special cases of the analysis provided in this paper. We also compare four networks which represent a wide spectrum of multistage interconnection networks. This study also illustrates how to determine optimal values for hardware parameters under different operating conditions. The simulations are done assuming random access pattern for the requests. It would be desirable to run the simulations using more realistic access patterns. The simulator that we have developed is adequate for such a study but the main difficulty lies in obtaining more realistic access patterns.

REFERENCES

- J. H. Patel, "Performance of processor-memory interconnections for multiprocessors," *IEEE Trans. on Computer*, vol. C-30, no. 10, pp. 771–780, Oct. 1981.
- [2] M. C. Pease, "The indirect binary n-cube microprocessor array," *IEEE Trans. on Computer*, vol. C-26, no. 5, pp. 458–473, May 1977.
- [3] D. H. Lawrie, "Access and alignment of data in an array processor," *IEEE Trans. on Computer*, vol. C-24, no 12, pp. 1145–1155, Dec. 1975.
- [4] A. Varma and C. S. Raghavendra., "Performance

analysis of a redundant path interconnection networks," *Proc. Int'l Conf. Parallel Processing*, pp. 474–479, Aug. 1985.

- [5] S. C. Kothari, G. M. Prabhu, and R. Roberts, "The Kappa network with fault-tolerant destination tag algorithm," *IEEE Trans. on Computer*, vol. 37, no. 5, pp. 612–617, May 1988.
- [6] S. C. Kothari, G. M. Prabhu, and R. Roberts, "Multipath network with cross link," *Journal of Parallel* and Distributed Computing, vol. 5, no. 2, pp. 185– 193, Apr. 1988.
- [7] D. M. Dias and J. R. Jump, "Analysis and simulation of buffered Delta networks," *IEEE Trans. on Computer*, vol. C-30, no. 4, pp. 273–282, Apr. 1981.
- [8] N. J. Davis, IV, and H. J. Siegel, "Performance study of multiple-packet multistage cube networks and comparison to circuit switching," *Proc. Int'l Conf. Parallel Processing*, pp. 108–114, Aug. 1986.
- [9] H. Yoon, K. Y. Lee, and M. T. Liu, "Performance analysis of multibuffered packet-wwitching networks in multiprocessor systems," *IEEE Trans. on Computer*, vol. 39, no. 3, pp. 319–327, Mar. 1990.
- [10] D. S. Parker and C. S. Raghavendra, "The Gamma network: a multiprocessor interconnection network with redundant paths," *9-th Int'l Symp. Computer Architecture*, pp. 73–80, May 1982.
- [11] M. Schwartz, *Telecommunication Networks: Pro*tocols, Modeling and Analysis. Massachusetts: Addison-Wesley Publishing Company, pp. 175-196, 1987.
- [12] J. Kim, "Design of multipath multistage interconnection networks and performance study of multiple-packet switching networks," MS thesis, Electrical Engineering and Computer Engineering, Iowa State University, 1988.
- [13] D. M. Dias and J. R. Jump, "Packet switching interconnection networks for modular systems," *IEEE Computer*, vol. 14, no. 12, pp. 43–53, Dec. 1981.

- [14] C. P. Kruskal and M. Snir, "The Performance of multistage interconnection networks for multiprocessors," *IEEE Trans. on Computer*, vol. 32, no. 12, pp. 1091–1098, Dec. 1983.
- [15] H. J. Siegel and R. J. McMillen, "The multistage cube: a versatile interconnection network," *Computer*, vol. 14, no. 12, pp. 65–76, Dec. 1981.

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