Lecture 07 Modeling and Optimization of VLSI Interconnects
(ECG 415/615 Introduction to VLSI System Design)

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Objectives

- Understand the importance of interconnects in VLSI systems
- Learn how interconnects scale
- Learn how interconnect delay and power are modeled
  - Resistance
  - Capacitance
  - Inductance
- Learn how interconnect delay and power are optimized at various levels
Interconnect Impact on Chip
Wire Models

All-inclusive model

Capacitance-only
Impact of Interconnect Parasitics

- Interconnect parasitics
  - reduce reliability
  - affect performance and power consumption

- Classes of parasitics
  - Capacitive
  - Resistive
  - Inductive
Nature of Interconnect

Local Interconnect

Global Interconnect

$S_{Local} = S_{Technology}$

$S_{Global} = S_{Die}$

Source: Intel
Readings

- H. B. Bakoglu, “Circuits interconnects and packaging for VLSI”, Addison Wesley
Components of VLSI system

- Logic
  - Functional Block
  - Logic Gates
  - Transistors

- Interconnects
  - Power/ground and Clock
  - Inter-block Signals
  - Intra-block Signals
Delay with technology scaling

This figure is from the ITRS Roadmap on interconnects.
Wire Delay

Today (i.e., 100nm):

\[ \tau_{RC} \approx 50\text{ps/mm} \]

Implies > 1 ns to traverse a 20mm x 20mm chip
This is a long time in a 2GHz processor
Wire Delay in the 35-nm Technology

- For the 35-nm technology generation using a copper conductor, a low-κ dielectric with κ=2, and a benchmark length $L = 1.0\text{ mm}$
  - the interconnects’ $RC$ response time is $\tau \approx 250\text{ ps}$.
  - In comparison, the switching delay or latency of a minimum-geometry 35-nm generation MOSFET is $\tau_d \approx 2.5\text{ ps}$.
Interconnect dimension trends in terms of IC generations

These figures are derived from *Design of High-Performance Microprocessor Circuits*, A. Chandrakasan, W. Bowhill, F. Fox, IEEE, 2001
## Trends in some integrated circuit parameters

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Local wiring pitch (nm)</td>
<td>210</td>
<td>150</td>
<td>105</td>
<td>50</td>
</tr>
<tr>
<td>Chip size at production (mm²)</td>
<td>310</td>
<td>310</td>
<td>310</td>
<td>310</td>
</tr>
<tr>
<td>Total interconnect length (m/cm²)</td>
<td>6879</td>
<td>11169</td>
<td>16063</td>
<td>33508</td>
</tr>
<tr>
<td>On-chip local clock (GHz)</td>
<td>3.990</td>
<td>6.739</td>
<td>11.511</td>
<td>28.751</td>
</tr>
<tr>
<td>Number of metal levels</td>
<td>9</td>
<td>10</td>
<td>10</td>
<td>11</td>
</tr>
<tr>
<td>Maximum power (W)</td>
<td>160</td>
<td>190</td>
<td>218</td>
<td>288</td>
</tr>
<tr>
<td>Package pin-count (high-performance)</td>
<td>2263</td>
<td>3012</td>
<td>4009</td>
<td>7100</td>
</tr>
</tbody>
</table>
Rent’s rule

- Rent’s rule relates the I/O requirement to the number of gates as:

\[ N_p = K_p N_g ^\beta \]

- As technology scales number of gates in a given area is increasing.
- More routing is required as technology scales.
Nature of the interconnect

These figures are derived from *Digital integrated circuit – a design perspective*, J. Rabaey Prentice Hall and a tutorial in SLIP by Dirk Stroobandt respectively.
Interconnect Topologies

Multi-sink

Multi-source

Bus or Routing Channel

A[0]

A[1]

A[63]

Grid
Modern interconnect

These figures are derived from Digital integrated circuit – a design perspective, J. Rabaey Prentice Hall and ITRS roadmap on interconnect respectively.
Multiple Interconnect Layers

IBM photomicrograph (SiO₂ has been removed)

Metal 2
M1/M2 via
Metal 1
Poly silicon
Diffusion

MOSFET (under polysilicon gate)
Interconnects are critical

- Chip Area Increasing.
- Average physical length increasing.
- Electrical length of interconnects increasing faster than physical length.
- Number of Interconnects increasing.
- Longer and more wires imply more delay (RC) and power ( $C_L V_{DD}^2 f$ )
Interconnect Solutions

- Design Methods - Timing Driven Floorplanning
- Devices - Improved $I_{dsat}$, Dual $V_t$
- Materials - Copper Interconnect, Low K Dielectric
- Geometries - Tall wires, Layers of metals, Shields
- Signaling Methods - Differential, Limited Swing
- Novel Methods - Wireless communication, Optical Interconnects
VLSI Design Cycle

- Chip Specs
  - Partitioning
    - Floorplan
      - RTL
  - Synthesis
    - Timing Analysis
      - Timing met
        - Layout
- Extraction
  - Timing Analysis
    - Timing met
      - Chip Tape out
Interconnect Focused Floorplanning

- Architectural Performance Sensitivity to Interconnect Delay
- Early Floorplanning
- Impact of New Circuit Techniques
- Interconnect-aware Architecture Design
Wire Models

- Why do we need models?
  - Models simplify analysis and simulation.
- Why model wires?
  - Estimate the delay due to wire.
  - Check for signal integrity and reliability.
- What are the implications of a wrong model?
  - Delay estimates can be wrong leading to slow or fast failures.
  - Might lead to over or under driving leading to power dissipation and reliability concerns.
Ideal Model

- Wires are lines on schematics having no electrical effect.
- A voltage change at one end appears at its other end without any delay i.e. wire is a equipotential region.
- Ideal model simplistic
  - Most wires connect local gates hence are short – Ideal model might be ok
  - For long i.e. global interconnects ideal model is absolutely wrong.
Early Models

- Wire width $\propto$ feature size
- Older technology had wide wires
- More cross-section area implies less resistance and more capacitance.
- Model wire only with capacitance
However...

- With scaling, width of wire reduced.
- Resistance of the wire no longer negligible.
- Wire not very long and a lumped RC is good enough approximation.
Interconnect Resistance

- Ohm’s Law: Resistance of wire $\propto$ wire length ($L$) and $1/\propto$ cross-section ($HW$)
- $\rho$ (resistivity) is the property of the material.

$$R = \frac{\rho L}{HW}$$
Sheet Resistance

- Wire height (H) is constant for a technology.
- Sheet resistance ($R_q$) is constant for each metal layer.
- Calculation of wire resistance is easy: multiply $R_q$ by $L/W$

\[ R = R_q \frac{L}{W} \]

with

\[ R_q = \frac{\rho}{H} \]
# Interconnect Resistance

<table>
<thead>
<tr>
<th>Material</th>
<th>$\rho$ ((\Omega\cdot m))</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silver (Ag)</td>
<td>$1.6 \times 10^{-8}$</td>
</tr>
<tr>
<td>Copper (Cu)</td>
<td>$1.7 \times 10^{-8}$</td>
</tr>
<tr>
<td>Gold (Au)</td>
<td>$2.2 \times 10^{-8}$</td>
</tr>
<tr>
<td>Aluminum (Al)</td>
<td>$2.7 \times 10^{-8}$</td>
</tr>
<tr>
<td>Tungsten (W)</td>
<td>$5.5 \times 10^{-8}$</td>
</tr>
</tbody>
</table>
Dealing with Resistance

- Selective Technology Scaling
- Use Better Interconnect Materials
  - reduce average wire-length
  - e.g. copper, silicides
- More Interconnect Layers
  - reduce average wire-length
Polycide Gate Mosfet

Silicides: WSi₂, TiSi₂, PtSi₂ and TaSi

Conductivity: 8-10 times better than Poly
# Sheet Resistance

<table>
<thead>
<tr>
<th>Material</th>
<th>Sheet Resistance (Ω/□)</th>
</tr>
</thead>
<tbody>
<tr>
<td>n- or p-well diffusion</td>
<td>1000 – 1500</td>
</tr>
<tr>
<td>$n^+, p^+$ diffusion</td>
<td>50 – 150</td>
</tr>
<tr>
<td>$n^+, p^+$ diffusion with silicide</td>
<td>3 – 5</td>
</tr>
<tr>
<td>$n^+, p^+$ polysilicon</td>
<td>150 – 200</td>
</tr>
<tr>
<td>$n^+, p^+$ polysilicon with silicide</td>
<td>4 – 5</td>
</tr>
<tr>
<td>Aluminum</td>
<td>0.05 – 0.1</td>
</tr>
</tbody>
</table>
Example: Intel 0.25 micron Process

5 metal layers
Ti/Al - Cu/Ti/TiN
Polysilicon dielectric

<table>
<thead>
<tr>
<th>LAYER</th>
<th>PITCH</th>
<th>THICK</th>
<th>A.R.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Isolation</td>
<td>0.67</td>
<td>0.40</td>
<td>-</td>
</tr>
<tr>
<td>Polysilicon</td>
<td>0.64</td>
<td>0.25</td>
<td>-</td>
</tr>
<tr>
<td>Metal 1</td>
<td>0.64</td>
<td>0.48</td>
<td>1.5</td>
</tr>
<tr>
<td>Metal 2</td>
<td>0.93</td>
<td>0.90</td>
<td>1.9</td>
</tr>
<tr>
<td>Metal 3</td>
<td>0.93</td>
<td>0.90</td>
<td>1.9</td>
</tr>
<tr>
<td>Metal 4</td>
<td>1.60</td>
<td>1.33</td>
<td>1.7</td>
</tr>
<tr>
<td>Metal 5</td>
<td>2.56</td>
<td>1.90</td>
<td>1.5</td>
</tr>
</tbody>
</table>

Layer pitch, thickness and aspect ratio
Interconnect Capacitance

- Capacitance of a wire = $f$ (Shape, Distance to surrounding wires, Distance to the substrate)
- Estimating Capacitance is a non-trivial task… subject of active research.
- To get an accurate estimate electric field solvers (2D or 3D) should be used.
- Solving fields is slow and will take ages for estimating capacitance of the whole chip.
- Various assumptions and approximations used to get quick estimates.
Area Capacitance

\[ C_{\text{int}} = \frac{\epsilon_{di}}{t_{di}} WL \]
<table>
<thead>
<tr>
<th>Material</th>
<th>$\varepsilon_r$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Free space</td>
<td>1</td>
</tr>
<tr>
<td>Aerogels</td>
<td>~1.5</td>
</tr>
<tr>
<td>Polyimides (organic)</td>
<td>3-4</td>
</tr>
<tr>
<td>Silicon dioxide</td>
<td>3.9</td>
</tr>
<tr>
<td>Glass-epoxy (PC board)</td>
<td>5</td>
</tr>
<tr>
<td>Silicon Nitride ($\text{Si}_3\text{N}_4$)</td>
<td>7.5</td>
</tr>
<tr>
<td>Alumina (package)</td>
<td>9.5</td>
</tr>
<tr>
<td>Silicon</td>
<td>11.7</td>
</tr>
</tbody>
</table>
Fringing Capacitance

\[ C_{wire} = C_{pp} + C_{fringe} = \frac{2\pi \varepsilon_{di}}{\log\left(\frac{t_{di}}{H}\right)} + \frac{w \varepsilon_{di}}{t_{di}} \]

\[ w \approx W - H/2 \]
Is this much of detail required… How to compute this?
Impact of Interwire Capacitance

(from [Bakoglu89])
# Wiring Capacitances (0.25 µm CMOS)

<table>
<thead>
<tr>
<th></th>
<th>Field</th>
<th>Active</th>
<th>Poly</th>
<th>A11</th>
<th>A12</th>
<th>A13</th>
<th>A14</th>
</tr>
</thead>
<tbody>
<tr>
<td>Poly</td>
<td>88</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>54</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A1</td>
<td>30</td>
<td>41</td>
<td>57</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>40</td>
<td>47</td>
<td>54</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A2</td>
<td>13</td>
<td>15</td>
<td>17</td>
<td>36</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>25</td>
<td>27</td>
<td>29</td>
<td>45</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A3</td>
<td>8.9</td>
<td>9.4</td>
<td>10</td>
<td>15</td>
<td>41</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>18</td>
<td>19</td>
<td>20</td>
<td>27</td>
<td>49</td>
<td></td>
<td></td>
</tr>
<tr>
<td>A4</td>
<td>6.5</td>
<td>6.8</td>
<td>7</td>
<td>8.9</td>
<td>15</td>
<td>35</td>
<td></td>
</tr>
<tr>
<td></td>
<td>14</td>
<td>15</td>
<td>15</td>
<td>18</td>
<td>27</td>
<td>45</td>
<td></td>
</tr>
<tr>
<td>A5</td>
<td>5.2</td>
<td>5.4</td>
<td>5.4</td>
<td>6.6</td>
<td>9.1</td>
<td>14</td>
<td>38</td>
</tr>
<tr>
<td></td>
<td>12</td>
<td>12</td>
<td>12</td>
<td>14</td>
<td>19</td>
<td>27</td>
<td>52</td>
</tr>
</tbody>
</table>
Orthogonal Capacitance

- Orthogonal capacitance is usually small
- May be necessary to compute sometimes for signal integrity issues.
Capacitance Crosstalk

- Capacitive coupling introduces crosstalk.
- Crosstalk slows down signals to static gates, can cause hard errors in storage nodes.
- Crosstalk can be controlled by methodological and optimization techniques.

5x5 μm Overlap: 0.35 V Interference
Coupling and Crosstalk

- Crosstalk current depends on capacitance, voltage ramp.
Crosstalk Analysis

- Assume worst-case voltage swings, signal slopes.
- Measure coupling capacitance based on geometrical alignment/overlap.
- Some nodes are particularly sensitive to crosstalk:
  - dynamic;
  - asynchronous.
Coupling Situations

better

worse

a x sig1 r

Layer-to-layer Coupling

- Long parallel runs on adjacent layers are also bad.
Methodological Solutions

- Add ground wires between signal wires:
  - coupling to $V_{SS}$, a stable signal, dominates;
  - can use $V_{SS}$ to distribute power, so long as power line is relatively stable.

- Extreme case—add ground plane. Costs an entire layer, may be overkill.
Ground Wires

\[ \begin{align*}
&\text{V}_{SS} \\
&\text{sig1} \\
&\text{V}_{SS} \\
&\text{sig2} \\
&\text{V}_{SS}
\end{align*} \]
Crosstalk and Signal Routing

- Can route wires to minimize required adjacency regions.
- Take advantage of natural holes in routing areas to decouple signals.
- Minimizes need for ground signals.
Crosstalk routing example

Channel:
Assumptions

- Take into account coupling only to wires in adjacent tracks.
- Ignore coupling of vertical wires.
- Assume that coupling/crosstalk is proportional to adjacency length.
Bad routing
Good routing
Multi-level Interconnection
The Lumped Model
Versions of Lumped Model

- A driver doesn’t see the total R or C of the wire.
- Versions of lumped model were used as good approximations.
Importance of Resistance

- Delay of wire $\propto$ to the resistance of the wire.
- Resistance means ohmic (IR) drop along the wire, reduces noise margin.
- IR drop a significant problem in the power lines where current density if high.
- Keep wires short, to reduce resistance.
- Contact resistance makes them vulnerable to electromigration.
How to Reduce Resistance?

- Materials with low resistivity (Cu).
- Reduce wire length – not always possible.
- Increase width – increases area and capacitance.
- Increase height – increases fringe capacitance.
- Provide bigger contacts, use less vias.
- Use metal instead of polysilicon even for short distance routing.
- Use silicide coating to reduce polysilicon resistance.
Accurate Estimate of Cap

- Accurate estimate of capacitance can be done for any geometry by using field solvers.
- Electric fields can be solved in 2D or 3D to accurately estimate the capacitance.
- Example field solver – FASTCAP
- Output usually being a capacitance matrix.
Estimate C Early in Design Cycle

- Imperative to estimate wire delay.
- Electric fields attenuate very fast.
- To calculate capacitance consider only near neighbors (both axes)
- A table of capacitance to ground per unit length for a given width can be created.
- Capacitance with horizontal neighbors depends on wire spacing.
Importance of Capacitance

- Delay of the wire is proportional to the capacitance charged.
- More capacitance means more dynamic power.
- Capacitance an increasing source of noise (coupling).
- Coupling make delay estimation hard.
How to Reduce Capacitance?

- Use low k dielectric which reduces permittivity and hence the capacitance.
- Increase the spacing between the wires (not always possible).
- Separate the two signals with a power or ground line (acting as shield).
- Use wire with minimum width wherever possible. (Increases resistance!)
Distributed model

- Wire can be modeled as a distributed RC line.

- As the number of elements increase distributed model becomes more accurate.

- For practical purposes wire-models with 5-10 elements are used to model the wire.
The Distributed RC-line

\[ \tau(V_{out}) = \frac{rc}{2} \frac{L^2}{2} \]
Step-response of RC Wire as a Function of Time and Space

![Graph showing the step-response of RC wire as a function of time and space with different markers indicating x = L/10, x = L/4, x = L/2, and x = L. The x-axis represents time in nsec, and the y-axis represents voltage in V.]
Step Response of Lumped and Distributed RC Networks:
Points of Interest.
Driving an RC-line

\[ \tau_D = R_s C_w + \frac{R_w C_w}{2} = R_s C_w + 0.5 r_w c_w L^2 \]

\[ t_p = 0.69 R_s C_w + 0.38 R_w C_w \]
Reducing RC-delay

Repeater

\[ M = L \frac{0.38rc}{t_{pbuf}} \]
Delay in distributed RC line

- Elmore analyzed the distributed model and came up with the figures for delay.

\[
\tau_N = \sum_{i=1}^{N} R_i \sum_{j=i}^{N} C_j = \sum_{i=1}^{N} C_i \sum_{j=1}^{i} R_j
\]

Elmore derived this equation in 1948 way before VLSI !!!
Elmore Delay...

- First order time constant at node is a sum of $RC$ components.
- All the upstream resistances are taken into account.
- Thus each node contributes to the delay.
- Amount of contribution is the product of the cap at the node and the amount of resistance from source to the node.
Generalized Elmore delay

\[ \int_{0}^{\infty} v_i(t) dt = \sum_{k=1}^{N} C_k V_k(0) R_{i,k} \]

with

\[ R_{i,k} = \sum_{j} R_j = \left( R_j \in \text{path}(i \rightarrow r) \cap \text{path}(k \rightarrow r) \right) \]

Rubinstein, Pinfield and Horowitz generalized Elmore delay

This figure is derived from Digital integrated circuit – a design perspective, J. Rabaey Prentice Hall
Inductance

- Early models didn’t include inductance.
- For VDSM Designs it cannot be ignored.
- Distributed RC model no longer accurate.
- Distributed RLC model should be used.
- Difficult to analyze… second order differential equations!!
LC coupling, self L and return R

(a) Victim

(b) Diagram with labels

These figures are derived from *Design of High-Performance Microprocessor Circuits*, A. Chandrakasan, W. Bowhill, F. Fox, IEEE, 2001
Inductive noise vs. line length

This figure is derived from *Design of High-Performance Microprocessor Circuits*, A. Chandrakasan, W. Bowhill, F. Fox, IEEE, 2001
Impact of signal returns on far-end

These figures are derived from *Design of High-Performance Microprocessor Circuits*, A. Chandrakasan, W. Bowhill, F. Fox, IEEE, 2001
Inductive Effects in Integrated Circuits

- Coaxial Cable
- Triplate Strip Line
- MicroStrip
- Wire above Ground Plane
Decoupling Capacitors

SUPPLY

Board Wiring

Chip

Bonding Wire

$C_d$

Decoupling Capacitor
The Transmission Line

\[ \frac{2}{\partial x^2} \frac{\partial^2 v}{\partial t^2} = r_c \frac{\partial v}{\partial t} + l_c \frac{\partial v}{\partial t} \]
Lossless Transmission Line - Parameters

Propagation Speed: Only a function of surrounding medium

\[ v = \frac{1}{\sqrt{lc}} = \frac{1}{\sqrt{\varepsilon \mu}} = \frac{c_0}{\sqrt{\varepsilon_r \mu_r}} \]

\[ t_f = \frac{1}{v} = \sqrt{lc} \]

\( \varepsilon: \) permittivity of insulator

\( \mu: \) permeability of insulator

Characteristic Impedance = Impedance presented by wire

\[ Z_0 = \frac{l}{\sqrt{c}} \]

100 to 500 Ω for typical wires
## Wave Propagation Speed

<table>
<thead>
<tr>
<th>Dielectric</th>
<th>$\varepsilon_r$</th>
<th>Propagation Speed (cm/nsec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vacuum</td>
<td>1</td>
<td>30</td>
</tr>
<tr>
<td>SiO$_2$</td>
<td>3.9</td>
<td>15</td>
</tr>
<tr>
<td>PC Board (Epoxy Glass)</td>
<td>5.0</td>
<td>13</td>
</tr>
<tr>
<td>Alumina (Ceramic Package)</td>
<td>9.5</td>
<td>10</td>
</tr>
</tbody>
</table>

Dielectric Constants and Wave Propagation Speeds for Various Materials, Used in Electronic Circuits (from [Bakoglu90]).
Wave Reflection for Different Terminations

Reflection Coefficient

\[
\rho = \frac{V_{\text{refl}}}{V_{\text{inc}}} = \frac{I_{\text{refl}}}{I_{\text{inc}}} = \frac{R-Z_0}{R+Z_0}
\]
Transmission Line Response \((R_L = \infty)\)

- \(R_S = 5Z_0\)
- \(R_S = Z_0\)
- \(R_S = Z_0/5\)

(a) \(V_{Dest}\)
(b) \(V_{Source}\)

\(t\) (in \(t_{light}\))
Lattice Diagram

\[ V_{\text{Source}} \xrightarrow{+ 0.8333} V_{\text{Dest}} \]

\[
\begin{align*}
0.8333 \text{ V} & \quad + 0.8333 \quad 1.6666 \text{ V} \\
2.2222 \text{ V} & \quad + 0.8333 \quad + 0.5556 \quad 2.7778 \text{ V} \\
3.1482 \text{ V} & \quad + 0.5556 \quad + 0.3704 \quad 3.5186 \text{ V} \\
3.7655 \text{ V} & \quad + 0.3704 \quad + 0.2469 \quad 4.0124 \text{ V} \\
\ldots & \quad + 0.2469
\end{align*}
\]

L/\nu \quad t
ECL Gate Line Response

![Circuit Diagram]

- \( V_{cc} \)
- \( V_{ee} \)
- \( V_{in} \)
- \( V_{ref} \)
- \( R_C \)
- \( R_B \)
- \( L = 2\text{cm} \)
- \( Z_0 = 100\Omega \)

(a)

![Graph]

- \( V_{out} \)
- \( t \) (nsec)
Output Buffer Model

\[ V_{DD} \]

\[ L = 10\text{nH} \]

\[ V_{in} \]

\[ L = 5\text{nH} \]

\[ Z_0 = 100 \]

\[ C_L = 5\text{pF} \]

\[ V_{out} \]

(a)

Clamping Diodes

\[ V_{DD} \]
Output Buffer - Response

CL = 25pF
RL = 100Ω
CL = 5pF
RL = 10kΩ
CL = 5pF
RL = 100Ω

(b)
When to Consider Transmission Line Effects?

- Transmission line effects should be considered when the rise or fall time of the input signal \((t_r, t_f)\) is smaller than the time-of-flight of the transmission line \((t_{flight})\).

**Rule of Thumb**

\[
t_r(t_f) < 2.5 t_{flight} = 2.5 \frac{L}{v}
\]
RI Introduced Noise
Power and Ground Distribution

- Must size wires to be able to handle current—requires designing topology of $V_{DD}/V_{SS}$ networks.
- Want to keep power network in metal—requires designing planar wiring.

(a) Finger-shaped network

(b) Network with multiple supply pins
Power distribution

Interdigitated power and ground lines

$V_{DD}$

$V_{SS}$
Power tree design

- Each branch must be able to supply required current to all of its subsidiary branches:

\[ I_x = \sum_{b \in x} I_b \]

- Trees are interdigitated to supply both sides of power supply.
Planar power/ground routing theorem

- Draw a dividing line through each cell such that all $V_{DD}$ terminals are on one side and all $V_{SS}$ terminals on the other.

- If floorplan places all cells with $V_{DD}$ on same side, there exists a routing for both $V_{DD}$ and $V_{SS}$ which does not require them to cross.
Planar routing theorem example
Power supply noise

- Variations in power supply voltage manifest themselves as noise into the logic gates.
- Power supply wiring resistance creates voltage variations with current surges.
- Voltage drops on power lines depend on dynamic behavior of circuit.
Tackling power supply noise

- Must measure current required by each block at varying times.
- May need to redesign power/ground network to reduce resistance at high current loads.
- Worst case, may have to move some activity to another clock cycle to reduce peak current.
Clock distribution

- Goals:
  - deliver clock to all memory elements with acceptable skew;
  - deliver clock edges with acceptable sharpness.
- Clocking network design is one of the greatest challenges in the design of a large chip.
Clock delay varies with position
H-tree
Clock distribution tree

- Clocks are generally distributed via wiring trees.
- Want to use low-resistance interconnect to minimize delay.
- Use multiple drivers to distribute driver requirements—use optimal sizing principles to design buffers.
- Clock lines can create significant crosstalk.
Clock distribution tree example