DATA AND COMPUTER COMMUNICATIONS

Lecture 3 Data Link Layer - Digital Data Communication Techniques

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Based on Lecture slides by William Stallings

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ASYNCHRONOUS AND SYNCHRONOUS TRANSMISSION

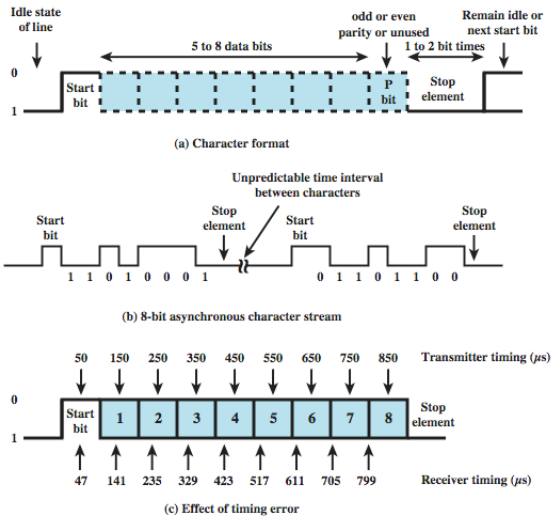
- timing problems require a mechanism to synchronize the transmitter and receiver
  - receiver samples stream at bit intervals
  - if clocks not aligned and drifting will sample at wrong time after sufficient bits are sent
- two solutions to synchronizing clocks
  - asynchronous transmission
  - synchronous transmission

asynchronous transmission	synchronous transmission
• *avoid timing problems by not sending long, uninterrupted streams of bits*	• a block of bits is transmitted in a steady stream without start and stop codes

Asynchronous Transmission

- data are transmitted one character at a time
  - each character is 5 to 8 bits in length
  - receiver has the opportunity to resynchronize at the beginning of each new character
- simple and cheap
  - requires overhead of 2 or 3 bits per character (~20%)
- the larger the block of bits, the greater the cumulative timing error
- good for data with large gaps (keyboard)

Asynchronous Transmission

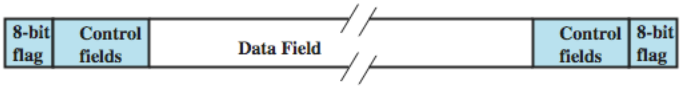


Asynchronous - Behavior

- simple
- cheap
- overhead of 2 or 3 bits per char (~20%)
- good for data with large gaps (keyboard)

Synchronous Transmission

- block of data transmitted sent as a frame
- clocks must be synchronized
  - can use separate clock line
  - or embed clock signal in data
- need to indicate start and end of block
  - use preamble and postamble
- more efficient (lower overhead) than async



Types of Error

- an error occurs when a bit is altered between transmission and reception
- single bit errors
  - only one bit altered
  - caused by white noise
- burst errors
  - contiguous sequence of *B* bits in which the first and last bits and any number of intermediate bits in error
  - caused by impulse noise or by fading in wireless
  - effect greater at higher data rates

Error Detection

- regardless of design you will have errors
- can detect errors by using an error-detecting code added by the transmitter
  - code is also referred to as *check bits*
- recalculated and checked by receiver
- still chance of undetected error
- parity
  - parity bit set so character has even (even parity) or odd (odd parity) number of ones
  - even number of bit errors goes undetected

ANALYSIS

Assume that data are transmitted in frames (F bits/frame).

Definition:

P_b: Probability that a bit is received in error; also known as the bit error rate (BER)

P_1: Probability that a frame arrives with no bit errors

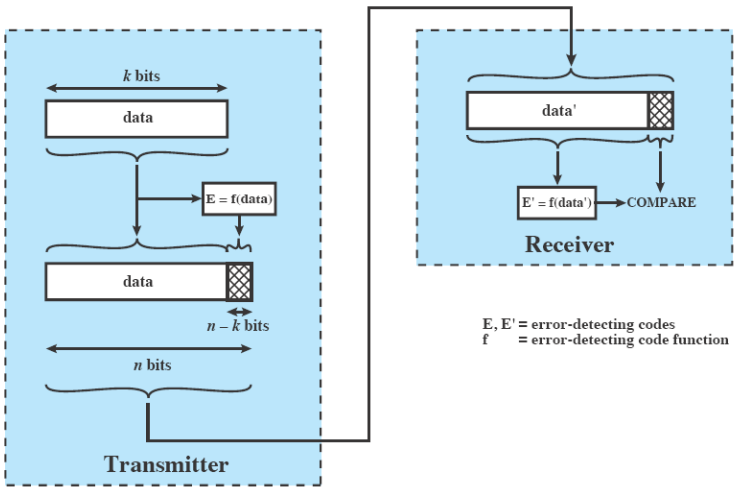
P_2: Probability that with an error-detecting algorithm in use, a frame arrives with one or more undetected errors

P_3: Probability that with an error-detecting algorithm in use, a frame arrives with one or more detected bit errors but no undetected bit errors

When no means are taken to detect errors

$P_3 = 0$, $P_1 = (1\text{-}P_b)^F$, $P_2 = 1\text{-}P_1$

ERROR DETECTION PROCESS



Parity Check

- the simplest error detecting scheme is to append a parity bit to the end of a block of data
  - Even parity – even number of 1s
    - Used for synchronous transmission
  - Odd parity – odd number of 1s
    - Used for asynchronous transmission
- if any even number of bits are inverted due to error, an undetected error occurs

Cyclic Redundancy Check

- one of most common and powerful checks
- for block of k bits transmitter generates an n-k bit frame check sequence (FCS)
- transmits n bits which is exactly divisible by some number
- receiver divides frame by that number
  - if no remainder, assume no error
  - for math, see Stallings chapter 6

Modulo 2 Arithmetic

- Modulo 2 arithmetic uses binary addition with no carries, which is just the exclusive-OR (XOR) operation.
- Definition:

T = n-bit frame to be transmitted

D = k-bit block of data, or message, the first k bits of T

F = (n-k)-bit FCS, the last (n-k) bits of T

P = pattern of n-k+1 bit $\frac{2^{n-k}D}{P} = Q + \frac{R}{P}$

Let $T = 2^{n-k}D + R$, where

Then $T/P = Q + R/P + R/P = Q$

Polynomials

- Express all values as polynomials in a dummy variable X with binary coefficients corresponding to the bits in the binary number $\frac{X^{n-k}D(X)}{P(X)} = Q(X) + \frac{R(X)}{P(X)}$

$$T(X) = X^{n-k}D(X) + R(X)$$

Selection of P(X)

- All single-bit errors, if P(X) has more than one nonzero term
- All double-bit errors, as long as P(X) is a primitive polynomial, with maximum exponent L, and the frame length is less than 2^L-1
- Any odd number of errors, as long as *P(X)* contains a factor $(X+1)$
- Any burst errors for which the length of the burst is $\leq n$-k, i.e., the length of the FCS
- A fraction $(1-2^{-(n-k-1)})$ of error bursts of length n-k+1
- A fraction $(1-2^{-(n-k)})$ of error bursts greater than

Selection of P(X)

- Four versions of *P(X)* are widely used

CRC-12 = $X^{12} + X^{11} + X^3 + X^2 + X + 1$

CRC-16 = $X^{16} + X^{15} + X^2 + 1$

CRC-CCITT = $X^{16} + X^{12} + X^5 + 1$

CRC-32 = $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$

DIGITAL LOGIC

- The CRC can be implemented as a dividing circuit consisting of XOR gates and a shift reg

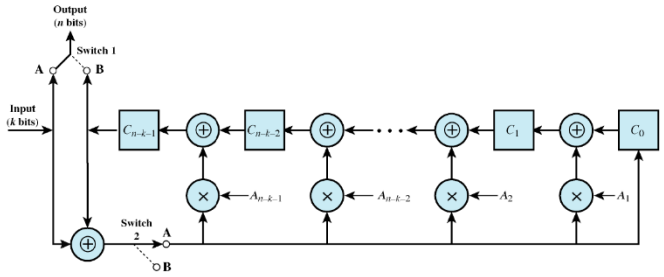
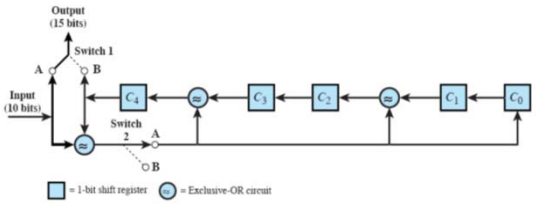


Figure 6.6 General CRC Architecture to Implement Divisor
$(1 + A_1X + A_2X^2 + \ldots + A_{n-1}X^{n-k-1} + X^{n-k})$

EXAMPLE

- Example: P(x) = X5 + X4 + X2 + 1



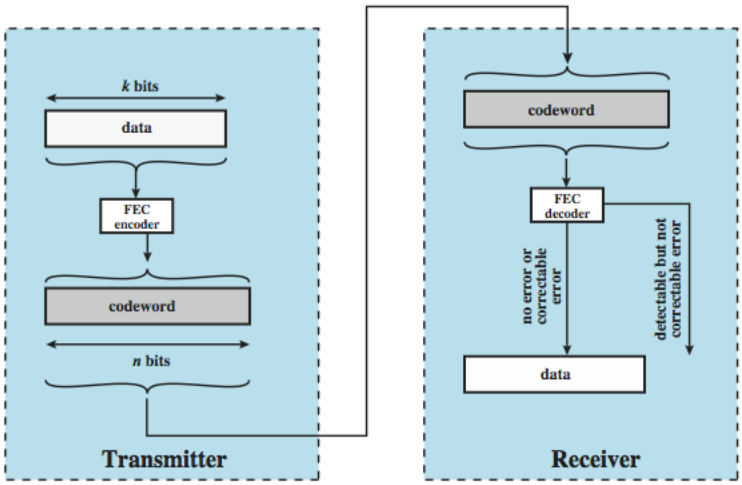
	C_4	C_3	C_2	C_1	C_0	$C_4 \approx C_3 \approx I$	$C_4 \approx C_1 \approx I$	$C_4 \approx I$	I = input	
Initial	0	0	0	0	0	1	1	1	1	
Step 1	1	0	1	0	1	1	1	1	0	
Step 2	1	1	1	1	1	1	1	0	1	
Step 3	1	1	1	1	0	0	0	1	0	
Step 4	0	1	0	0	1	1	0	0	0	Message to be sent
Step 5	1	0	0	1	0	1	0	1	0	
Step 6	1	0	0	0	1	0	0	0	1	
Step 7	0	0	0	1	0	1	0	1	1	
Step 8	1	0	0	0	1	1	1	1	0	
Step 9	1	0	1	1	1	0	1	0	1	
Step 10	0	1	1	1	0					

(b) Example with input of 1010001101

Error Correction

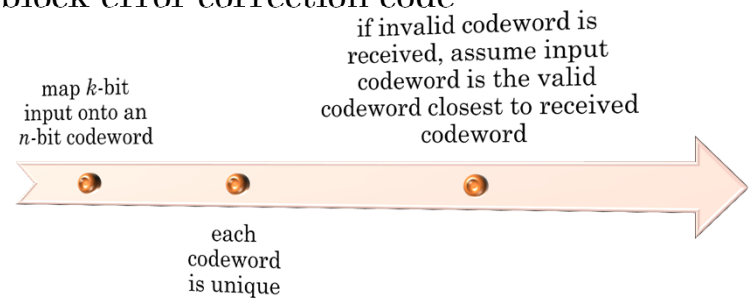
- correction of detected errors usually requires data block to be retransmitted
- not appropriate for wireless applications
  - bit error rate is high causing lots of retransmissions
  - when propagation delay long (satellite) compared with frame transmission time, resulting in retransmission of frame in error plus many subsequent frames
- need to correct errors on basis of bits received
- codeword
  - on the transmission end each k-bit block of data is mapped into an n-bit block (n > k) using a forward error correction (FEC) encoder

Error Correction Process



How Error Correction Works

- adds redundancy to transmitted message
- can deduce original despite some errors
- means have reduced effective data rate
- eg. block error correction code



Block Code Principles

- Hamming distance $d(v_1, v_2)$ between two n-bit binary sequences v_1 and v_2 is the number of bits in which v_1 and v_2 disagree
- The design of a block code is equivalent to the design of a function of the form $v_c=f(v_d)$, where v_d is a vector of k data bits and v_c is a vector of n codeword bits
- Redundancy of the code: $(n-k)/k$
- Code rate: k/n

Block Code Principles

- For a code consisting of the codewords w_1, w_2, …, w_s, where $s=2^n$,

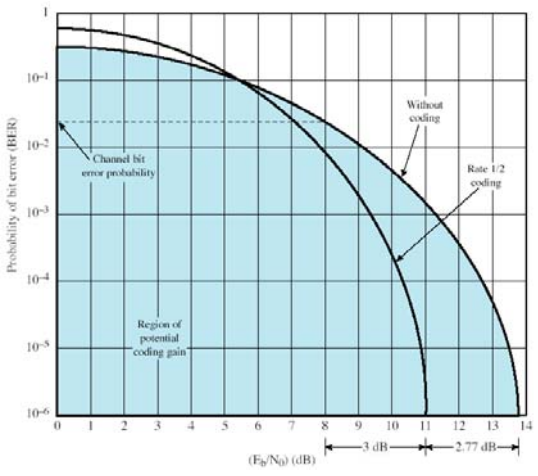
$$d_{\min} = \min_{i \neq j} [d(w_i, w_j)]$$

- The maximum number of guaranteed correctable errors per codeword

$$t = \left\lfloor \frac{d_{\min} - 1}{2} \right\rfloor$$

- The maximum number of guaranteed detectable errors per codeword
- $t=d_{min}$-1

How Coding Improves Performance



Line Configuration - Topology

topology

- refers to the physical arrangement of stations

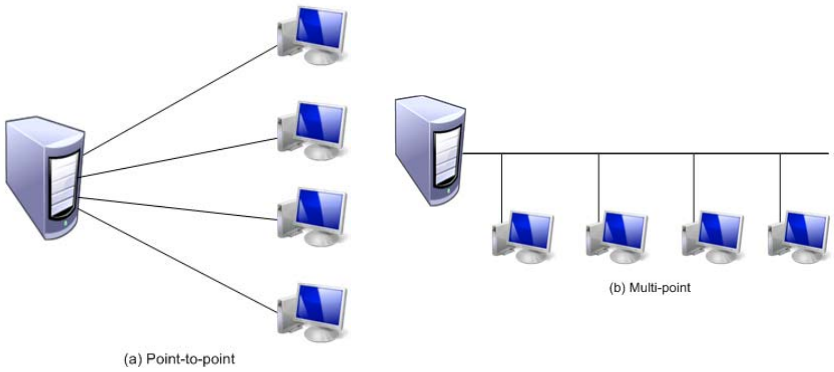
point to point - two stations

- such as between two routers / computers

multi point - multiple stations

- traditionally mainframe computer and terminals
- now typically a local area network (LAN)

Line Configuration - Topology



Line Configuration - Duplex

- classify data exchange as half or full duplex
- half duplex (two-way alternate)
  - only one station may transmit at a time
  - requires one data path
- full duplex (two-way simultaneous)
  - simultaneous transmission and reception between two stations
  - requires two data paths
    - separate media or frequencies used for each direction
  - or echo canceling

Summary

- asynchronous & synchronous transmission
  - asynchronous
    - data transmitted one character at a time
  - synchronous
    - block of bits transmitted in steady stream without start and stop codes
- error detection and correction
  - single bit error and error burst
  - error detecting codes
    - parity and cyclic redundancy check (CRC)
- line configurations
  - topology
  - full duplex and half duplex