

EE292: Fundamentals of ECE

Fall 2012

TTh 10:00-11:15 SEB 1242

Lecture 27

121101

<http://www.ee.unlv.edu/~b1morris/ee292/>

Final Exam Details

- Tuesday 12/11 at 10:10 am
- Exam is inclusive of the entire course
 - Extra emphasis on untested material
- No Calculators
- You are allowed 2 pages of handwritten notes

New Material

- Chapter 7 – Digital Logic
 - Number representation
 - 2's complement arithmetic
 - Combinatorial Logic
 - Basic gates (AND, OR, NOT)
 - Truth table
 - Boolean algebra
 - De Morgan's Laws
 - Synthesis of logic (SOP, POS)
 - Sequential Logic
 - Flip-flops (SR, D, JK, clocked and edge triggered)
 - Registers (digital word representation, shift-register)
- Chapter 12 – Transistors
 - Operating modes (NMOS, PMOS)
 - CMOS logic gates

Midterm 2

- Chapter 10 – Diodes
 - Ideal and Offset Model
- Chapter 4 – Transient Analysis
 - Steady-State Analysis
 - 1st-Order Circuits
- Chapter 5 – Steady-State Sinusoidal Analysis
 - RMS Values
 - Phasors
 - Complex Impedance
 - Circuit Analysis with Complex Impedance

Midterm 1

- Chapter 1 – Intro to Circuits
 - Current, voltage, power, energy
 - KCL, KVL
 - Ohm's Law
- Chapter 2 – Resistive Circuits
 - Series/parallel resistance
 - Voltage/current divider
 - Node-voltage (super nodes)
 - Mesh-current (super mesh)
 - Superposition
 - Thevenin and Norton equivalents
- Chapter 3 – Inductance and Capacitance
 - IV relationships, power/energy
 - Series and parallel equivalents

Positional Notation for Numbers

- Base B number \rightarrow B symbols per digit
 - Base 10 (Decimal): 0, 1, 2, 3, 4, 5, 6, 7, 8, 9
 - Base 2 (binary) 0, 1
- Number representation
 - $d_{N-1}d_{N-2} \dots d_2d_1d_0$ is N digit number
 - 2^N different numbers can be represented
 - Value = $d_{N-1} \times B^{N-1} + d_{N-2} \times B^{N-2} + \dots + d_1 \times B^1 + d_0 \times B^0$
- Examples
 - (Decimal): 90
 - = $9 \times 10^1 + 0 \times 10^0$
 - (Binary): 1011010
 - = $1 \times 2^6 + 0 \times 2^5 + 1 \times 2^4 + 1 \times 2^3 + 0 \times 2^2 + 1 \times 2^1 + 0 \times 2^0$
 - = $64 + 16 + 8 + 2$
 - = 90
 - 7 binary digits needed for 2 digit decimal number

Binary Arithmetic

- Addition in binary is the same as with decimal
 - Only have 2 values (0, 1) in binary

		Sum	Carry
0 + 0	=	0	0
0 + 1	=	1	0
1 + 1	=	0	1
1 + 1 + 1	=	1	1

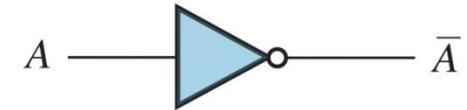
- 2's complement for subtraction
 - $-x = \bar{x} + 1$

Basic Logic Gates

- Inverter – NOT operation or complement of a variable
 - $\text{NOT}(A) = \bar{A}$

A	\bar{A}
0	1
1	0

(a) Truth table



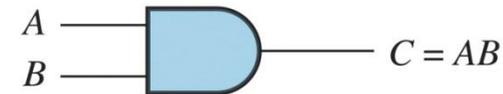
(b) Symbol for an inverter

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- AND - computes the logical multiplication of input variables
 - $\text{AND}(A, B) = AB$

A	B	$C = AB$
0	0	0
0	1	0
1	0	0
1	1	1

(a) Truth table



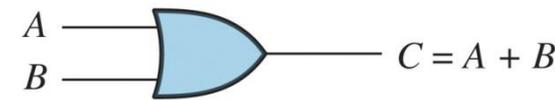
(b) Symbol for two-input AND gate

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- OR - computes the logical addition of input variables
 - $\text{OR}(A, B) = A + B$

A	B	$C = A + B$
0	0	0
0	1	1
1	0	1
1	1	1

(a) Truth table



(b) Symbol for two-input OR gate

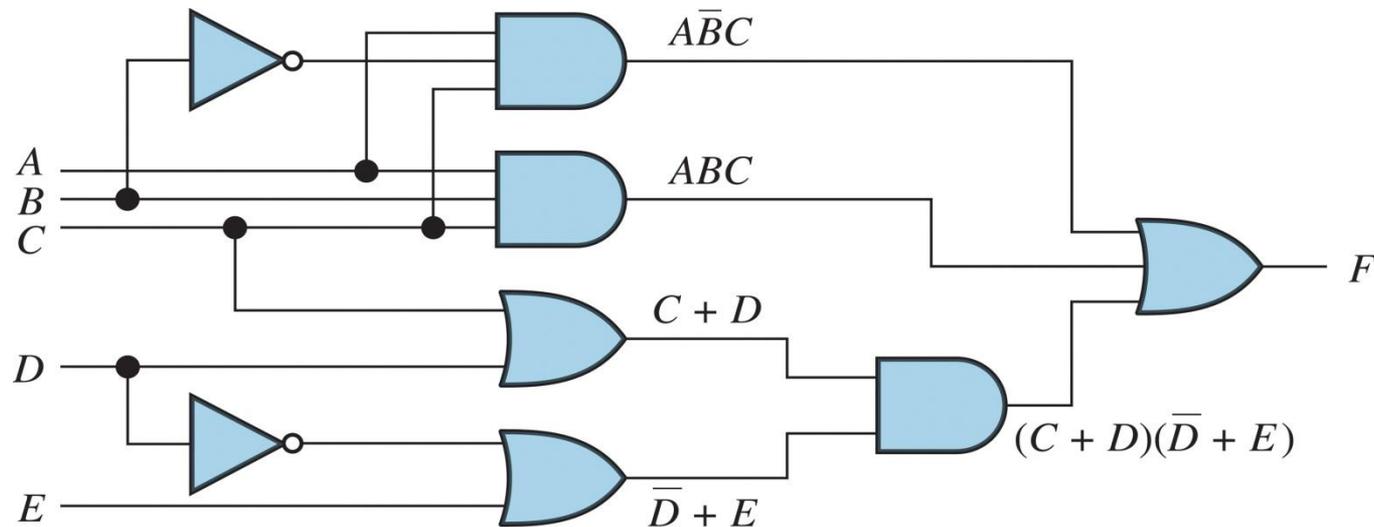
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Boolean Algebra

- Mathematical theory of logical variables
- Use basic AND, OR, and NOT relationships to prove a Boolean expression
 - Can generate a truth table to specify the output relationship for all possible input values
- De Morgan's Laws
 - Provides a way to convert an AND relationship into an OR relationship and vice versa
 - $ABC = \overline{\overline{A} + \overline{B} + \overline{C}}$
 - $(A + B + C) = \overline{\overline{A}\overline{B}\overline{C}}$

Implementation of Boolean Expressions

- A logical variable can be composed of Boolean relationships
 - AND, OR, NOT, etc.
- Gate level implementation is straightforward
- Example
- $F = A\bar{B}C + ABC + (C + D)(\bar{D} + E)$



Simplifying Boolean Expression

- Find simpler equivalent expressions by manipulation of equation and Boolean relations
- Example
- $F = A\bar{B}C + ABC + (C + D)(\bar{D} + E)$
- $F = A\bar{B}C + ABC + (C\bar{D} + CE + D\bar{D} + DE)$
- $F = A\bar{B}C + ABC + (C\bar{D} + CE + 0 + DE)$
- $F = AC(\bar{B} + B) + (C\bar{D} + CE + 0 + DE)$
- $F = AC(1) + (C\bar{D} + CE + 0 + DE)$
- $F = C(A + \bar{D} + E) + DE$

Sum-of-Products Implementation

- Find all output rows that have a 1 output
 - Determine AND relationship between inputs
- OR the AND terms from each row

<i>A</i>	<i>B</i>	<i>C</i>	<i>D</i>		AND Term
0	0	0	1		$\bar{A}\bar{B}\bar{C}$
0	0	1	0		
0	1	0	1		$\bar{A}B\bar{C}$
0	1	1	0		
1	0	0	0		
1	0	1	0		
1	1	0	1		$AB\bar{C}$
1	1	1	1		ABC

$$D = \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + AB\bar{C} + ABC$$

Product-of-Sums Implementation

- Find all output rows that have a 0 output
 - Determine OR relationship between inputs
- AND the OR terms from each row

<i>A</i>	<i>B</i>	<i>C</i>	<i>D</i>		OR Term
0	0	0	1		
0	0	1	0		$A + B + \bar{C}$
0	1	0	1		
0	1	1	0		$A + \bar{B} + \bar{C}$
1	0	0	0		$\bar{A} + B + C$
1	0	1	0		$\bar{A} + B + \bar{C}$
1	1	0	1		
1	1	1	1		

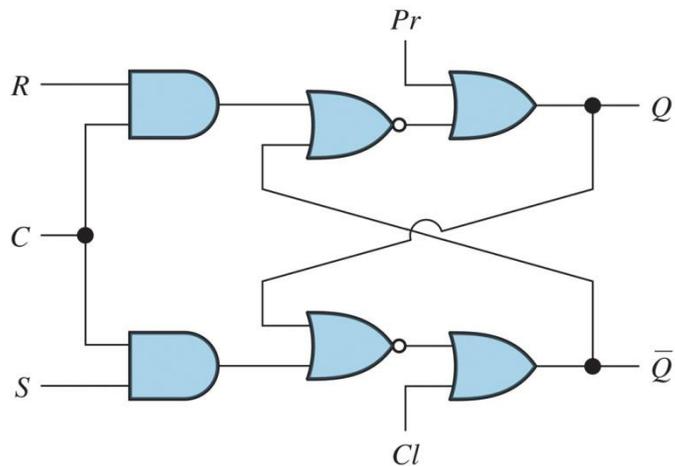
$$D = (A + B + \bar{C})(A + \bar{B} + \bar{C})(\bar{A} + B + C)(\bar{A} + B + \bar{C})$$

Sequential Logic

- Combinatorial logic output is only dependent on input at the given time
- Sequential logic has outputs that are dependent not only on current input but past input as well
 - The circuits have “memory”
- Often times sequential circuits use a clock signal to regulate when the output should change
 - These are called synchronous circuits
 - Asynchronous circuits are able to change as soon as inputs change (no clock signal is required)

Clocked SR with Asynchronous Input

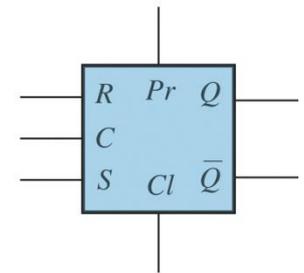
- Clocked set and reset functionality with asynchronous preset (Pr) and clear (Cl)



(a) Circuit diagram

Pr	Cl	R	S	C	Q_n
0	0	0	0	×	Q_{n-1}
0	0	0	1	1	1
0	0	1	0	1	0
×	×	1	1	1	Not allowed
0	1	×	×	×	0
1	0	×	×	×	1
1	1	×	×	×	Not allowed

(b) Truth table

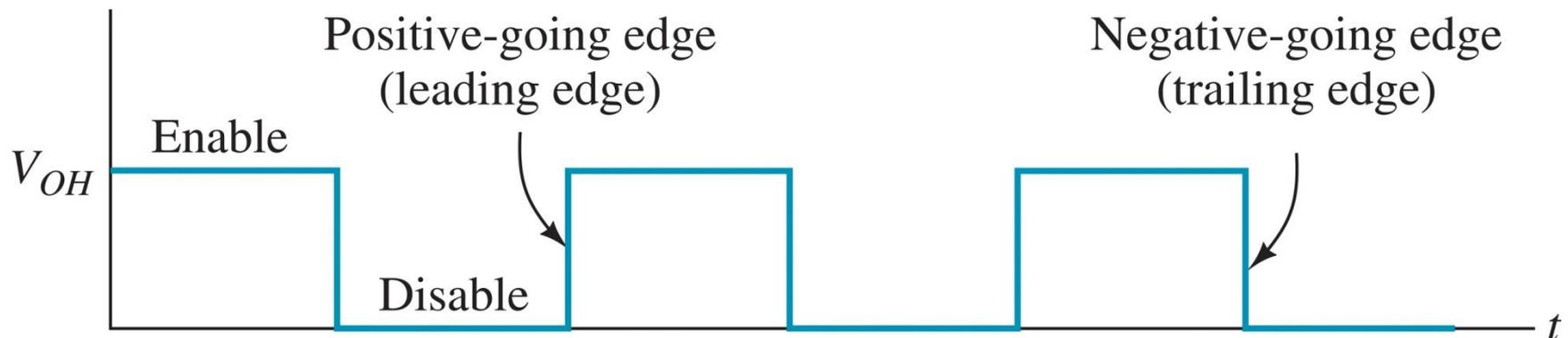


(c) Circuit symbol

- Add OR gates at $Q\bar{Q}$ outputs to automatically set or reset state
 - Notice that the clocked S and R cannot be high at the same time and neither can the asynchronous preset Pr and clear Cl

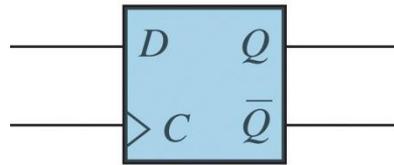
Edge-Triggered Circuits

- The clocked SR flip-flop uses the clock signal as an enable signal
 - When the clock is high the circuit is allowed to change
- Edge-triggered circuits only respond at the time when the clock changes between low and high
 - Positive-edge-triggered – low to high transition
 - Known as the leading edge
 - Negative-edge-triggered – high to low transition
 - Known as the trailing edge



D Flip-Flop

- The delay (D) flip-flop is edge-triggered to take make the output the same as the input right before the clock transition



(a) Circuit symbol

C	D	Q_n
0	×	Q_{n-1}
1	×	Q_{n-1}
↑	0	0
↑	1	1

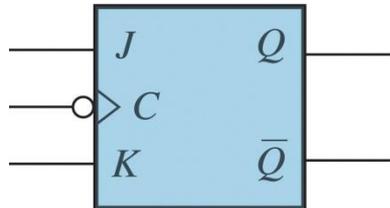
(b) Truth table

indicates a transition
from low to high

- The triangle by the clock signal C indicates it is positive-edge-triggered
 - Up arrow in truth table indicates rising edge

JK Flip-Flop

- Similar operation to the SR flip-flop
 - Except when J and K are both high, the output state Q will toggle



(a) Circuit symbol

C	J	K	Q_n	Comment
0	×	×	Q_{n-1}	Memory
1	×	×	Q_{n-1}	Memory
↓	0	0	Q_{n-1}	Memory
↓	0	1	0	Reset
↓	1	0	1	Set
↓	1	1	\bar{Q}_{n-1}	Toggle

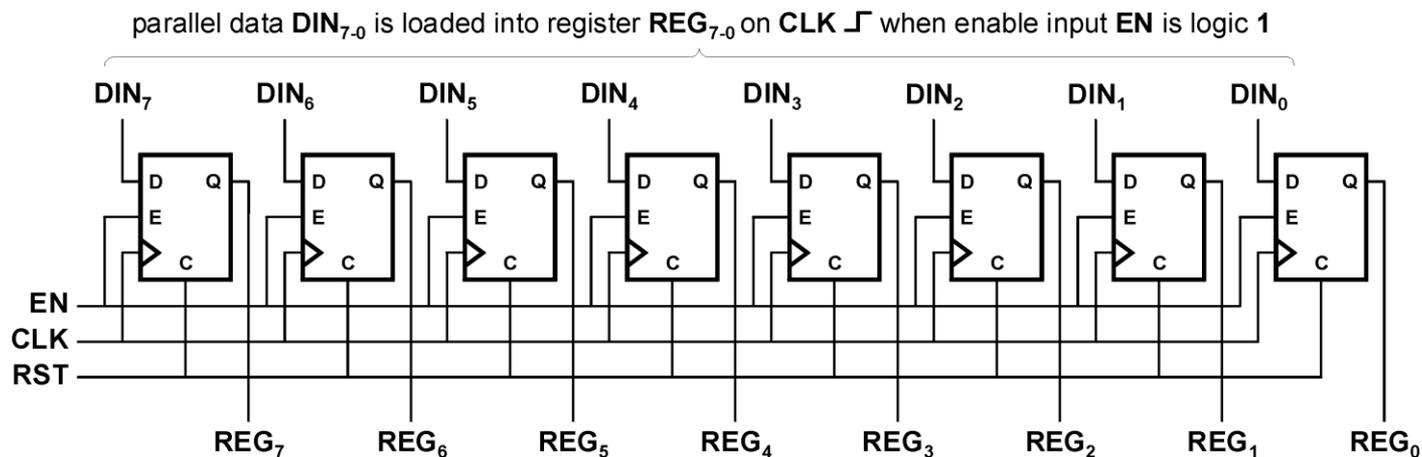
(b) Truth table

indicates a transition
from low to high

- Notice this is a negative-edge-triggered
 - Triangle with a preceding invert bubble

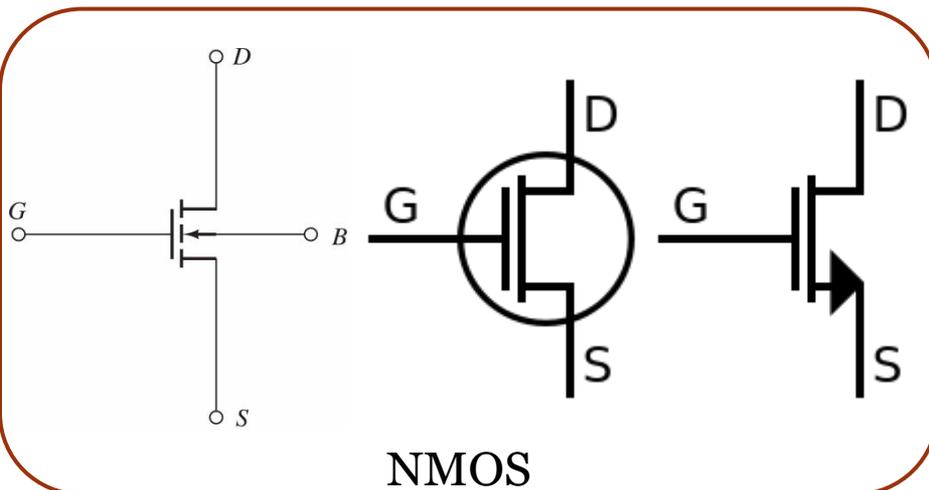
Registers

- A flip-flop is able to store a single bit
- A register is an array of flip-flops used to store a digital word
 - A hexadecimal number requires 4 bits so 4 flip-flops are required to internally store the hex number

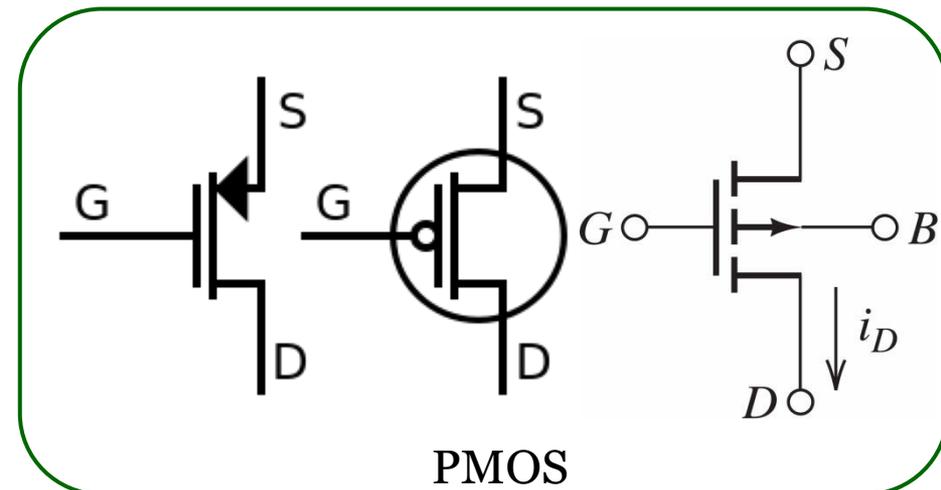


NMOS and PMOS Transistors

- NMOS
 - n-channel device → electrons carry charge into device
 - Current flows in from drain (out of source)
- Circuit symbol
 - Body arrow pointing to gate
 - Arrow pointing out from source

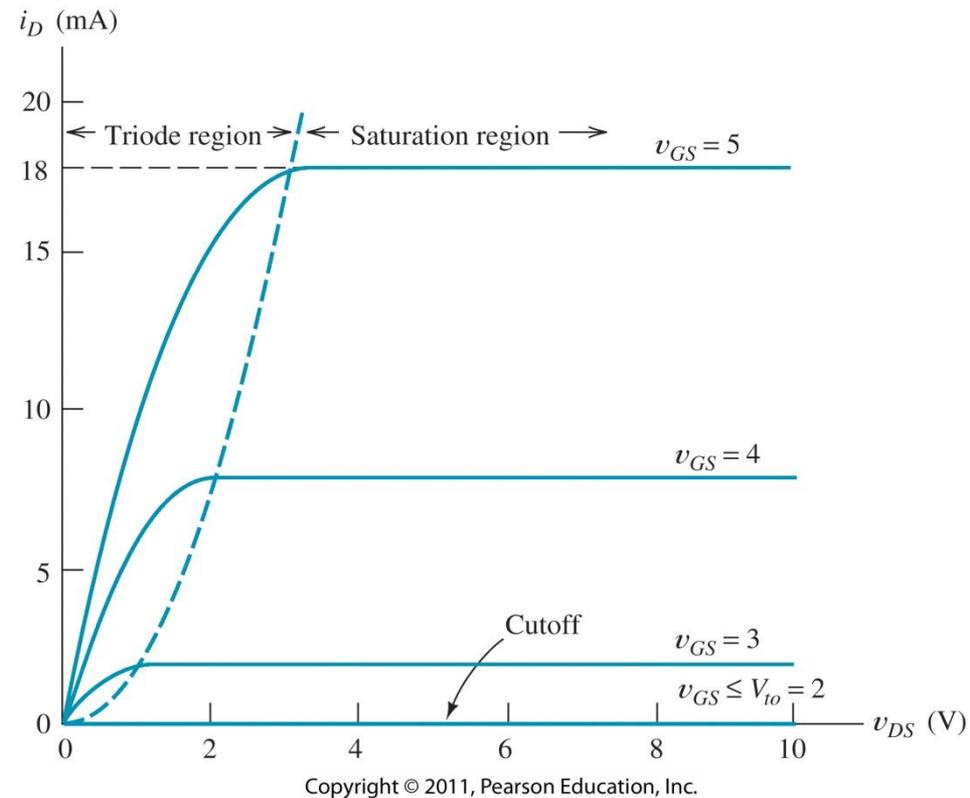


- PMOS
 - p-channel device → “holes” carry positive charge
 - Current flows out of drain (in from source)
- Circuit symbol
 - Body arrow pointing away from gate
 - Arrow pointing in from source
 - Invert bubble on the gate



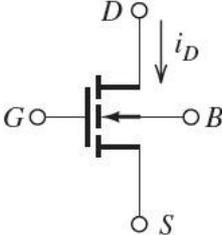
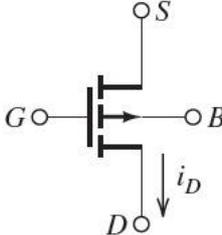
Transistor Operation

- Cutoff region
 - No drain current when gate voltage is below a threshold
 - $i_D = 0$ for $v_{GS} \leq V_{to}$
- Triode (linear) region
 - Transistor behaves like a resistor
 - $v_{DS} < v_{GS} - V_{to}$ and $v_{GS} \geq V_{to}$
- Saturation region
 - Constant current operation
 - $v_{DS} \geq v_{GS} - V_{to}$ and $v_{GS} \geq V_{to}$
- Above definitions for NMOS, PMOS has the same I/V characteristics but the signs of the voltages are inverted



MOSFET Summary

Table 12.1. MOSFET Summary

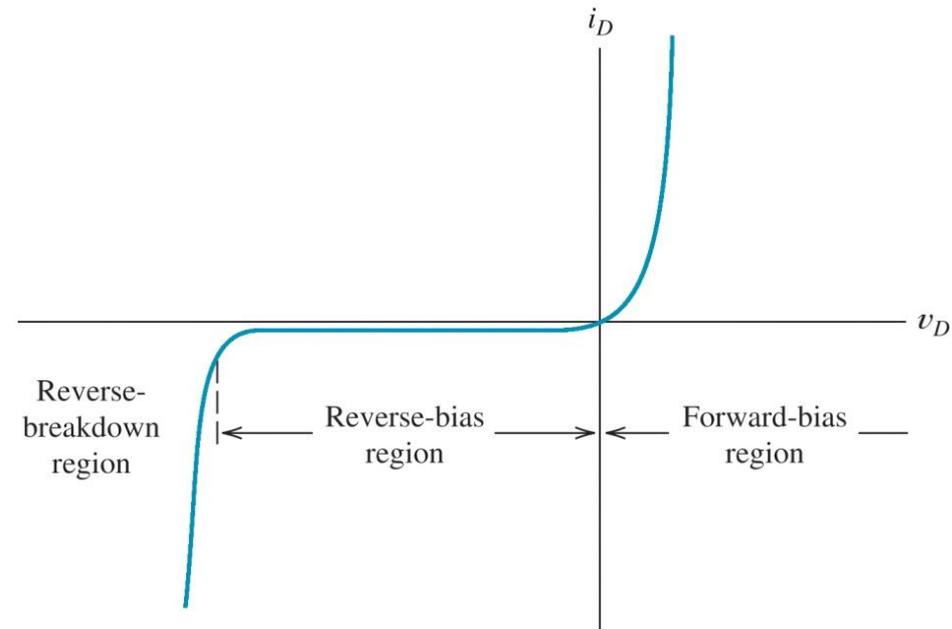
	NMOS	PMOS
Circuit symbol		
KP (typical value)	$50 \mu\text{A}/\text{V}^2$	$25 \mu\text{A}/\text{V}^2$
K	$(1/2) KP (W/L)$	$(1/2) KP (W/L)$
V_{to} (typical value)	+1 V	-1 V
Cutoff region	$v_{GS} \leq V_{to}$ $i_D = 0$	$v_{GS} \geq V_{to}$ $i_D = 0$
Triode region	$v_{GS} \geq V_{to}$ and $0 \leq v_{DS} \leq v_{GS} - V_{to}$ $i_D = K [2(v_{GS} - V_{to}) v_{DS} - v_{DS}^2]$	$v_{GS} \leq V_{to}$ and $0 \geq v_{DS} \geq v_{GS} - V_{to}$ $i_D = K [2(v_{GS} - V_{to}) v_{DS} - v_{DS}^2]$
Saturation region	$v_{GS} \geq V_{to}$ and $v_{DS} \geq v_{GS} - V_{to}$ $i_D = K (v_{GS} - V_{to})^2$	$v_{GS} \leq V_{to}$ and $v_{DS} \leq v_{GS} - V_{to}$ $i_D = K (v_{GS} - V_{to})^2$
v_{DS} and v_{GS}	Normally assume positive values	Normally assume negative values

CMOS Logic Gates

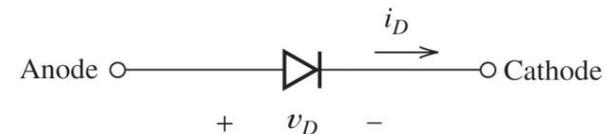
- Logic gates composed of complementary metal-oxide semiconductor (CMOS) transistors
 - Both NMOS and PMOS transistors utilized in circuits
- With CMOS it is easy to build fundamental gates
 - E.g. NAND and NOR
- MOS operation is simplified with logic levels
 - The transistor is a voltage controlled switch
 - Either in cutoff or saturation
 - Cutoff = “off” = open switch
 - NMOS gate voltage low, PMOS gate voltage high
 - Saturation = “on” = closed switch
 - NMOS gate voltage high, PMOS gate voltage low

Diode Voltage/Current Characteristics

- Forward Bias (“On”)
 - Positive voltage v_D supports large currents
 - Modeled as a battery (0.7 V for offset model)
- Reverse Bias (“Off”)
 - Negative voltage \rightarrow no current
 - Modeled as open circuit
- Reverse-Breakdown
 - Large negative voltage supports large negative currents
 - Similar operation as for forward bias



(b) Volt–ampere characteristic

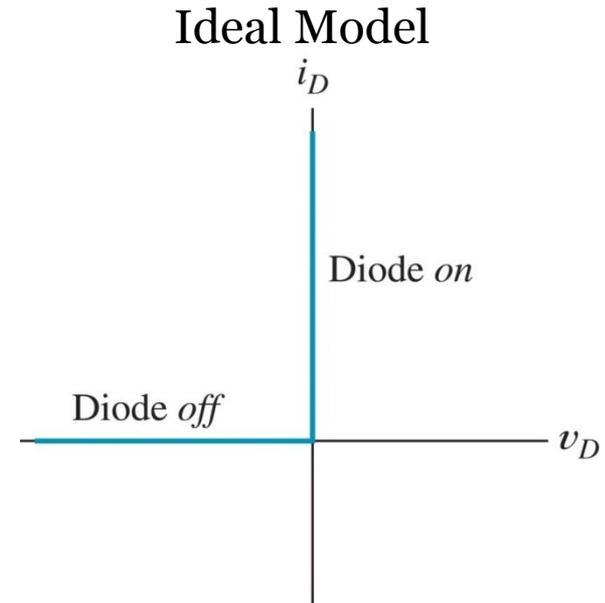


(a) Circuit symbol

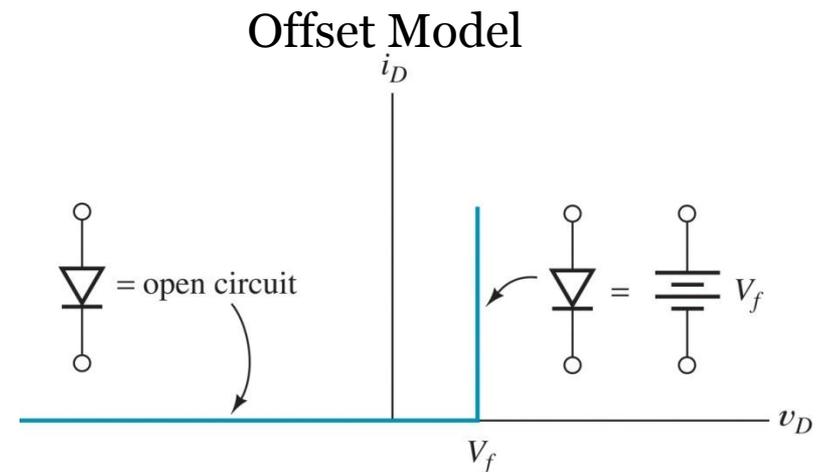
Diode Models

- Ideal model – simple
- Offset model – more realistic

- Two state model
- “On” State
 - Forward operation
 - Diode conducts current
 - Ideal model → short circuit
 - Offset model → battery
- “Off” State
 - Reverse biased
 - No current through diode → open circuit



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Circuit Analysis with Diodes

- Assume state {on, off} for each ideal diode and check if the initial guess was correct
 - $i_d > 0$ positive for “on” diode
 - $v_d < v_{on}$ for “off” diode
 - These imply a correct guess
 - Otherwise adjust guess and try again
- Exhaustive search is daunting
 - 2^n different combinations for n diodes
- Will require experience to make correct guess

DC Steady-State Analysis

- Analysis of C, L circuits in DC operation
 - Steady-state – non-changing sources
- Capacitors $i = C \frac{dv}{dt}$
 - Voltage is constant \rightarrow no current \rightarrow open circuit
- Inductors $v = L \frac{di}{dt}$
 - Current is constant \rightarrow no voltage \rightarrow short circuit
- Use steady-state analysis to find initial and final conditions for transients

General 1st-Order Solution

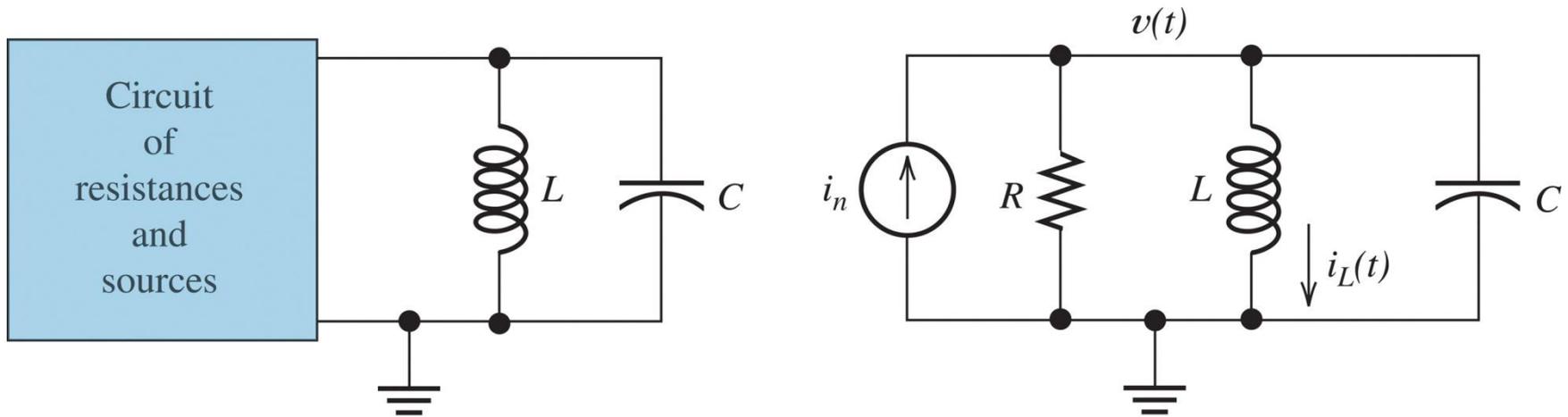
- Both the current and voltage in an 1st-order circuit has an exponential form
 - RC and LR circuits

- The general solution for current/voltage is:

$$x(t) = x_f + [x(t_0^+) - x_f] e^{-(t-t_0)/\tau}$$

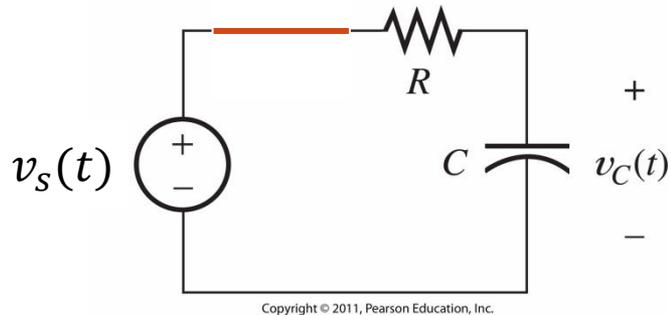
- x – represents current or voltage
 - t_0 – represents time when source switches
 - x_f - final (asymptotic) value of current/voltage
 - τ – time constant (RC or $\frac{L}{R}$)
 - Transient is essentially zero after 5τ
- Find values and plug into general solution
 - Steady-state for initial and final values
 - Two-port equivalents for τ

Example Two-Port Equivalent



- Given a circuit with a parallel capacitor and inductor
 - Use Norton equivalent to make a parallel circuit equivalent
- Remember:
 - Capacitors add in parallel
 - Inductors add in series

RC/RL Circuits with General Sources



- $RC \frac{dv_c(t)}{dt} + v_c(t) = v_s(t)$
 - The solution is a differential equation of the form
 - $\tau \frac{dx(t)}{dt} + x(t) = f(t)$
 - Where $f(t)$ the forcing function
 - The full solution to the diff equation is composed of two terms
 - $x(t) = x_p(t) + x_h(t)$
- $x_p(t)$ is the particular solution
 - The response to the particular forcing function
 - $x_p(t)$ will be of the same functional form as the forcing function
 - $f(t) = e^{st} \rightarrow x_p(t) = Ae^{st}$
 - $f(t) = \cos(\omega t) \rightarrow x_p(t) = A\cos(\omega t) + B\sin(\omega t)$
 - $x_h(t)$ is the homogeneous solution
 - “Natural” solution that is consistent with the differential equation for $f(t) = 0$
 - The response to any initial conditions of the circuit
 - Solution of form
 - $x_h(t) = Ke^{-t/\tau}$

Second-Order Circuits

- RLC circuits contain two energy storage elements
 - This results in a differential equation of second order (has a second derivative term)
- Use circuit analysis techniques to develop a general 2nd-order differential equation of the form

$$\frac{di^2(t)}{dt^2} + 2\alpha \frac{di(t)}{dt} + \omega_0^2 i(t) = f(t)$$

- Use KVL, KCL and I/V characteristics of inductance and capacitance to put equation into standard form
- Must identify α , ω_0 , $f(t)$

Useful I/V Relationships

- Inductor

- $v(t) = L \frac{di(t)}{dt}$

- $i(t) = \frac{1}{L} \int_{t_0}^t v(t) dt + i(t_0)$

- Capacitor

- $i(t) = C \frac{dv(t)}{dt}$

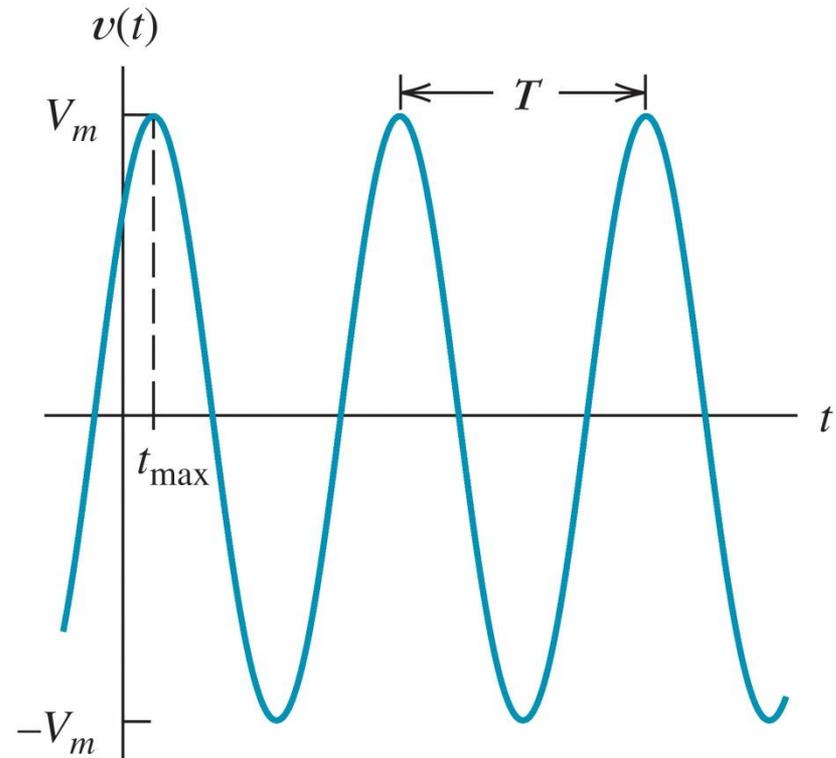
- $v(t) = \frac{1}{C} \int_{t_0}^t i(t) dt + v(t_0)$

Steady-State Sinusoidal Analysis

- In Transient analysis, we saw response of circuit network had two parts
 - $x(t) = x_p(t) + x_h(t)$
- Natural response $x_h(t)$ had an exponential form that decays to zero
- Forced response $x_p(t)$ was the same form as forcing function
 - Sinusoidal source \rightarrow sinusoidal output
 - Output persists with the source \rightarrow at steady-state there is no transient so it is important to study the sinusoid response

Sinusoidal Currents and Voltages

- Sinusoidal voltage
 - $v(t) = V_m \cos(\omega_0 t + \theta)$
 - V_m - peak value of voltage
 - ω_0 - angular frequency in radians/sec
 - θ - phase angle in radians
- This is a periodic signal described by
 - T - the period in seconds
 - $\omega_0 = \frac{2\pi}{T}$
 - f - the frequency in Hz = 1/sec
 - $\omega_0 = 2\pi f$



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- Note: Assuming that θ is in degrees, we have
 - $t_{\max} = -\theta/360 \times T$.

Root-Mean-Square Values

- $$P_{avg} = \frac{\left[\sqrt{\frac{1}{T} \int_0^T v^2(t) dt} \right]^2}{R}$$

- Define rms voltage

- $$V_{rms} = \sqrt{\frac{1}{T} \int_0^T v^2(t) dt}$$

$$P_{avg} = \frac{V_{rms}^2}{R}$$

- Similarly define rms current

- $$I_{rms} = \sqrt{\frac{1}{T} \int_0^T i^2(t) dt}$$

$$P_{avg} = I_{rms}^2 R$$

RMS Value of a Sinusoid

- Given a sinusoidal source

- $v(t) = V_m \cos(\omega_0 t + \theta)$

- $$V_{rms} = \sqrt{\frac{1}{T} \int_0^T v^2(t) dt}$$

$$V_{rms} = \sqrt{\frac{1}{T} \int_0^T V_m^2 \cos^2(\omega_0 t + \theta) dt}$$

using $\cos^2(x) = 1/2 + 1/2 \cos(2x)$

$$= \sqrt{\frac{V_m^2}{2T} \int_0^T [1 + \cos(2\omega_0 t + 2\theta)] dt}$$

⋮

$$= \frac{V_m}{\sqrt{2}}$$

- The rms value is an “effective” value for the signal

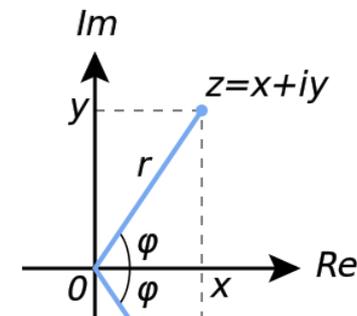
- E.g. in homes we have 60Hz 115 V rms power

- $V_m = \sqrt{2} \cdot V_{rms} = 163 V$

Conversion Between Forms

- Rectangular to polar form
- $r^2 = x^2 + y^2$
- $\tan\theta = \frac{y}{x}$
- Polar to rectangular form
- $x = r\cos\theta$
- $y = r\sin\theta$
- Convert to polar form
- $z = 4 - j4$
- $r = \sqrt{4^2 + 4^2} = 4\sqrt{2}$
- $\theta = \arctan\left(\frac{y}{x}\right) = \arctan(-1) = -\frac{\pi}{4}$
- $z = 4\sqrt{2}e^{-j\pi/4}$

x (degrees)	x (radians)	$\sin(x)$	$\cos(x)$	$\tan(x)$
0	0	0	1	0
15	$\frac{\pi}{12}$	$\frac{-1 + \sqrt{3}}{2\sqrt{2}}$	$\frac{1 + \sqrt{3}}{2\sqrt{2}}$	$2 - \sqrt{3}$
30	$\frac{\pi}{6}$	$\frac{1}{2}$	$\frac{\sqrt{3}}{2}$	$\frac{1}{\sqrt{3}}$
45	$\frac{\pi}{4}$	$\frac{1}{\sqrt{2}}$	$\frac{1}{\sqrt{2}}$	1
60	$\frac{\pi}{3}$	$\frac{\sqrt{3}}{2}$	$\frac{1}{2}$	$\sqrt{3}$
75	$\frac{5\pi}{12}$	$\frac{1 + \sqrt{3}}{2\sqrt{2}}$	$\frac{-1 + \sqrt{3}}{2\sqrt{2}}$	$2 + \sqrt{3}$
90	$\frac{\pi}{2}$	1	0	<i>NaN</i>

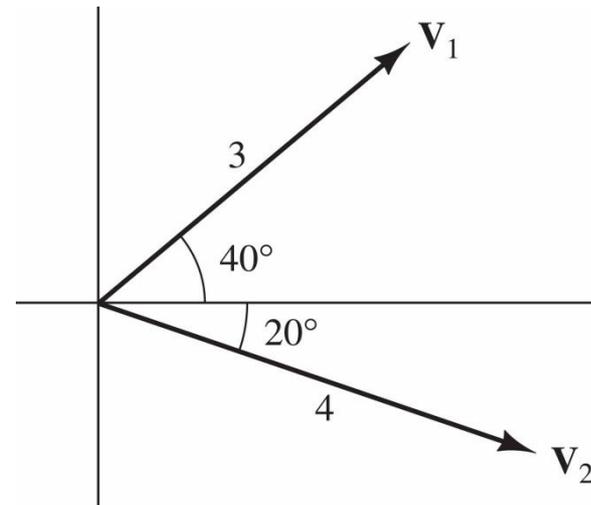


Source: Wikipedia

Phasors

- A representation of sinusoidal signals as vectors in the complex plane
 - Simplifies sinusoidal steady-state analysis
- Given
 - $v_1(t) = V_1 \cos(\omega t + \theta_1)$
- The phasor representation is
 - $\mathbf{V}_1 = V_1 \angle \theta_1$
- For consistency, use only cosine for the phasor
 - $v_2(t) = V_2 \sin(\omega t + \theta_2) = V_2 \cos(\omega t + \theta_2 - 90^\circ)$
 - $\mathbf{V}_2 = V_2 \angle (\theta_2 - 90^\circ)$

- Phasor diagram



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- $\mathbf{V}_1 = 3 \angle (40^\circ)$
- $\mathbf{V}_2 = 4 \angle (-20^\circ)$
- Phasors rotate counter clockwise
 - \mathbf{V}_1 leads \mathbf{V}_2 by 60°
 - \mathbf{V}_2 lags \mathbf{V}_1 by 60°

Complex Impedance

- Impedance is the extension of resistance to AC circuits
 - Extend Ohm's Law to an impedance form for AC signals
 - $V = ZI$
- Inductors oppose a change in current
 - $Z_L = \omega L \angle \left(\frac{\pi}{2}\right) = j\omega L$
 - Current lags voltage by 90°
- Capacitors oppose a change in voltage
 - $Z_C = \frac{1}{\omega C} \angle \left(-\frac{\pi}{2}\right) = -j \frac{1}{\omega C} = \frac{1}{j\omega C}$
 - Current leads voltage by 90°
- Resistor impedance the same as resistance
 - $Z_R = R$

Circuit Analysis with Impedance

- KVL and KCL remain the same
 - Use phasor notation to setup equations
- Replace sources by phasor notation
- Replace inductors, capacitors, and resistances by impedance value
 - This value is dependent on the source frequency ω
- Use your favorite circuit analysis techniques to solve for voltage or current
 - Reverse phasor conversion to get sinusoidal signal in time

Current and Voltage

- Current – the flow of charge
 - $i(t) = \frac{dq(t)}{dt}$
 - Must define a reference direction
 - The direction positive charge flows
- Voltage – the potential difference between 2 circuit nodes
 - The polarity defines the reference

Power and Energy

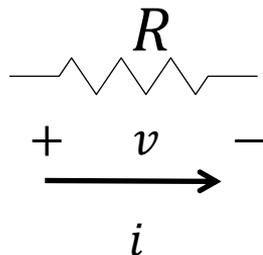
- Power – rate of energy transfer
 - $p(t) = v(t)i(t)$
 - Defined for passive reference configuration
 - Current flows into positive polarity terminal
- Energy – amount of power delivered in time interval
 - $w = \int_{t_1}^{t_2} p(t)dt$
- $p, w > 0 \rightarrow$ energy absorbed by element
- $p, w < 0 \rightarrow$ energy supplied by element

Ohm's Law and Resistance

- Ohm's Law
 - $v = iR$
- Resistance
 - $R = \frac{v}{i}$
 - Units of Ohms Ω
- Series equivalent
 - $R_{\Sigma} = R_{eq} = \sum_i R_i$
- Parallel equivalent
 - $R_{eq} = \frac{1}{\sum_i \frac{1}{R_i}}$

$$\begin{aligned}
 p &= vi \\
 &= i^2 R \\
 &= \frac{V^2}{R} = GV^2
 \end{aligned}$$

$$v = iR$$

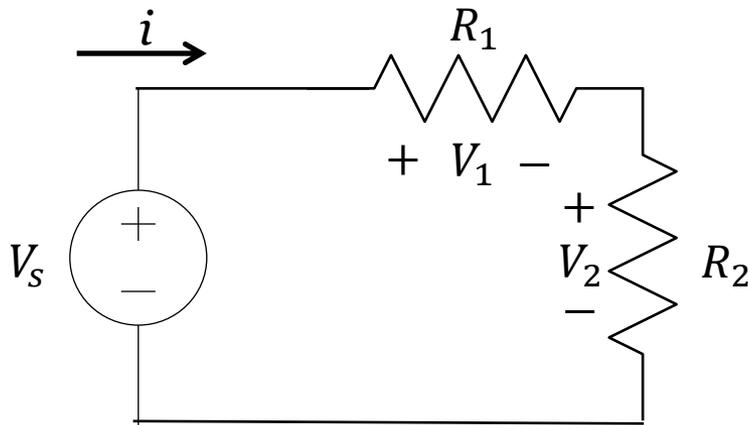


Kirchhoff's Laws

- KCL :
 - conservation of charge
 - sum of currents entering node is equal current leaving node
- KVL :
 - conservation of energy
 - Sum of voltages in circuit loop is zero

Voltage-Division Principle

- The fraction of voltage across a given resistance in a series connection is the ratio of the given resistance to the total series resistance

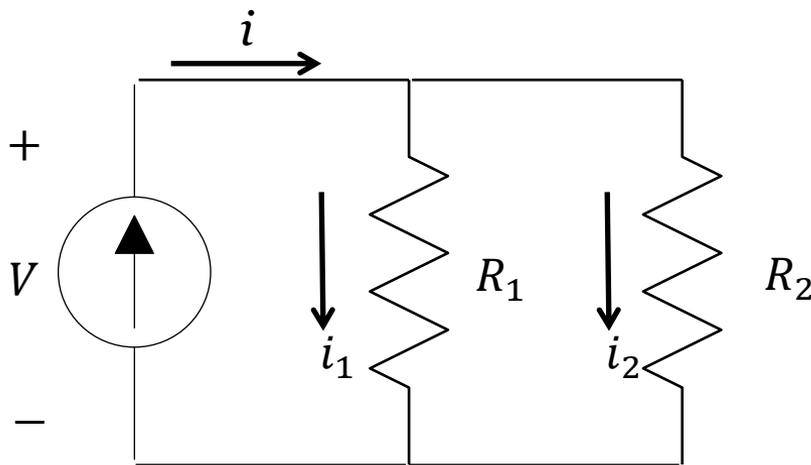


The larger resistor \rightarrow more voltage drop across it

$$\begin{aligned} v_1 &= iR_1 & v_2 &= iR_2 \\ &= V_s \left(\frac{R_1}{R_1 + R_2} \right) & &= V_s \left(\frac{R_2}{R_1 + R_2} \right) \end{aligned}$$

Current-Division Principle

- The fraction of current flowing in a given resistance is the ratio of the other resistance to the sum of the two resistances
 - Only applies for parallel pairs



$$i_1 = \frac{v}{R_1} = \frac{i}{R_1} \left(\frac{R_1 R_2}{R_1 + R_2} \right) \quad i_2 = \frac{v}{R_2}$$

$$= \left(\frac{R_2}{R_1 + R_2} \right) i \quad = \left(\frac{R_1}{R_1 + R_2} \right) i$$

Smaller the resistor \rightarrow more current through parallel path

Node-Voltage Analysis

- Voltages at nodes are unknown
- Use KCL equations at nodes
- Steps:
 1. Select a reference node
 2. Label each additional by a node voltage
 3. Write network equations
 - Use KCL at nodes/supernodes, KVL for any additional equations
 - A supernode is required when a voltage source is not grounded
 - Dependent source equations should be re-written in terms of node voltages
 4. Put the equations into standard form and solve for the node voltages

Mesh-Current Analysis

- Currents around a “mesh” are unknown
 - Requires planar (non-overlapping) circuits
- Use KVL equations around a mesh

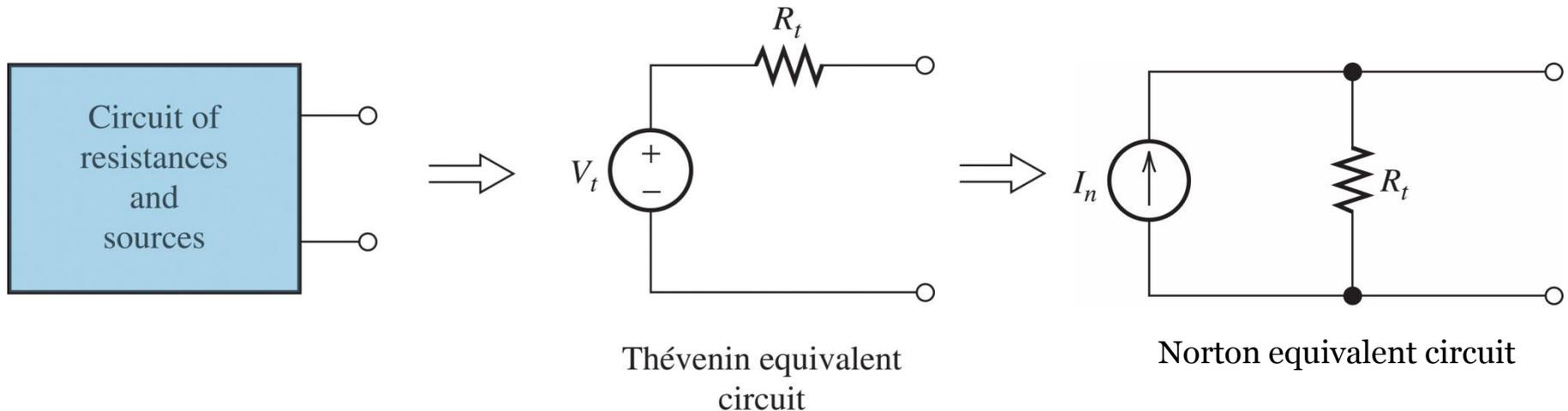
- Steps:
 1. Define mesh currents clockwise around “minimum” loops
 2. Write network KVL equations for each mesh current
 - Define current sources in terms of mesh currents
 - Shared current sources require a supermesh
 - Dependent source equations should be re-written in terms of mesh currents
 3. Put the equations into standard form and solve for the node voltages

Superposition Principle

- Given a circuit with multiple independent sources, the total response is the sum of the responses to each individual source
 - Requires linear dependent sources
- Analyze each independent source individually
 - Must zero out independent sources, but keep dependent sources
 - A voltage source becomes a short circuit
 - A current source becomes an open circuit



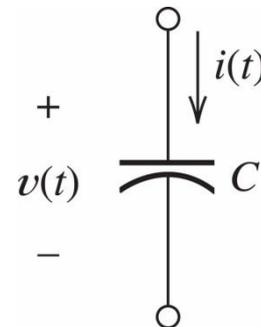
Thevenin/Norton Equivalent Circuit



- View circuit from two terminals
 - Thévenin equivalent circuit consists of a voltage source in series with a resistance
 - Norton equivalent circuit consists of a current source in parallel with a resistance
- We care about three things
 - Open circuit voltage
 - Short circuit current
 - Equivalent resistance (same value for both)
- It is possible to switch between Thevenin and Norton easily

Capacitance

- Circuit property to deal with energy in electric fields
- Capacitor stores charge and creates an electric field
 - $q = Cv$
 - $i = C \frac{dv}{dt}$
 - $v = \frac{1}{C} \int_{t_0}^t i(t) dt + v(t_0)$
- Power
 - $p(t) = v(t) i(t)$
 - $= v(t) C \frac{dv}{dt}$
- Energy
 - $w(t) = \frac{1}{2} Cv^2(t)$
- Capacitances in parallel
 - Add like resistors in series
- Capacitances in series
 - Behave like resistors in parallel
- Be sure to remember passive reference configuration



Inductance

- Circuit property to deal with energy in magnetic fields
- Inductors store energy in a magnetic field
 - $v(t) = L \frac{di}{dt}$
 - $i(t) = \frac{1}{L} \int_{t_0}^t v(t) dt + i(t_0)$
- Power
 - $p(t) = v(t) i(t)$
 - $= L \frac{di}{dt} i(t)$
- Energy
 - $w(t) = \frac{1}{2} Li^2(t)$
- Inductances in series
 - Add like resistors in series
- Inductances in parallel
 - Behave like resistors in parallel
- Be sure to remember passive reference configuration

