EE292: Fundamentals of ECE

Fall 2012
TTh 10:00-11:15 SEB 1242

Lecture 26
121128

http://www.ee.unlv.edu/~b1morris/ee292/

Outline

- Review
  - Transistors
- CMOS Logic Gates
- Project Info
  - Website
  - Arduino

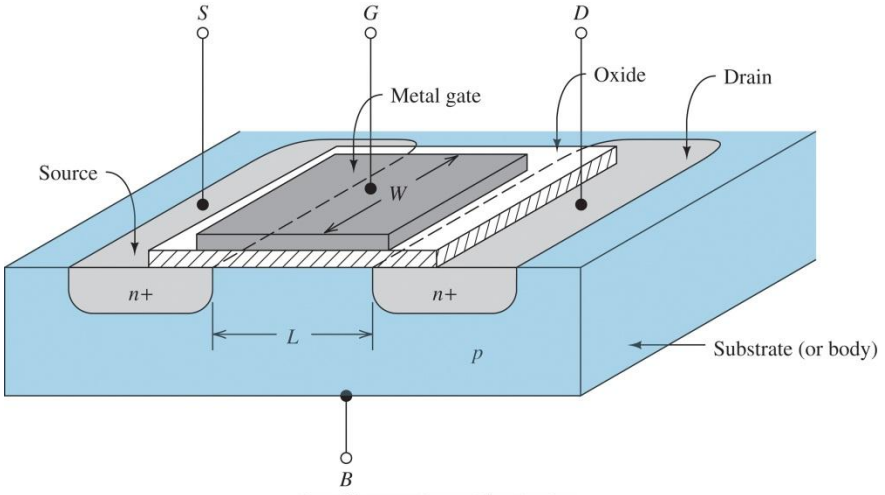
Transistor

- Very important device used in amplifiers and logic gates
- Metal-oxide-semiconductor field-effect transistor (MOSFET) is the key device that has propelled our rapid technology growth
  - Can be easily fabricated on silicon wafers
  - Small area which enables large numbers of transistors on a chip and faster processing
  - Cheap

  - Insulated-gate field-effect transistor (IGFET) is the more general term for today's transistors

Physical Transistor

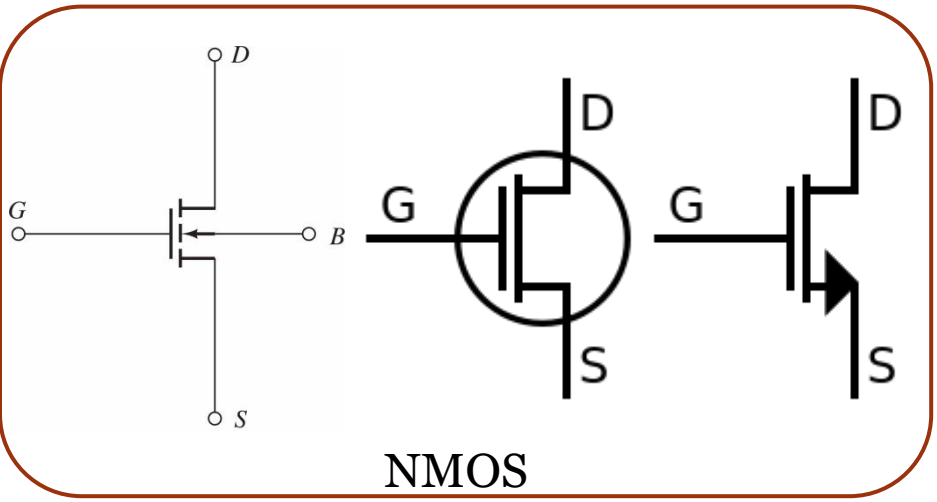
- A MOSFET transistor is a 4 terminal device that is fabricated on the surface of a silicon wafer
- 4 terminals
  - (D)rain
  - (G)ate
  - (S)ource
  - (B)ody or substrate
- Body is often tied to the source to make a 3 terminal device
- When voltage is applied on the gate and voltage is applied between the drain and source
  - Current flows into the drain and out the source terminal
  - Amount of current is controlled by the gate voltage

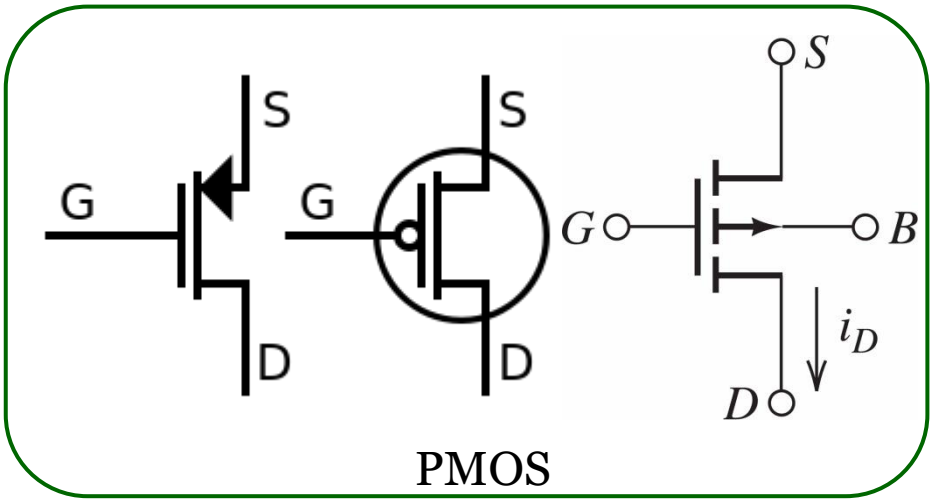


NMOS and PMOS Transistors

- NMOS
  - n-channel device → electrons carry charge into device
  - Current flows in from drain (out of source)
- Circuit symbol
  - Body arrow pointing to gate
  - Arrow pointing out from source

- PMOS
  - p-channel device → "holes" carry positive charge
  - Current flows out of drain (in from source)
- Circuit symbol
  - Body arrow pointing away from gate
  - Arrow pointing in from source
  - Invert bubble on the gate

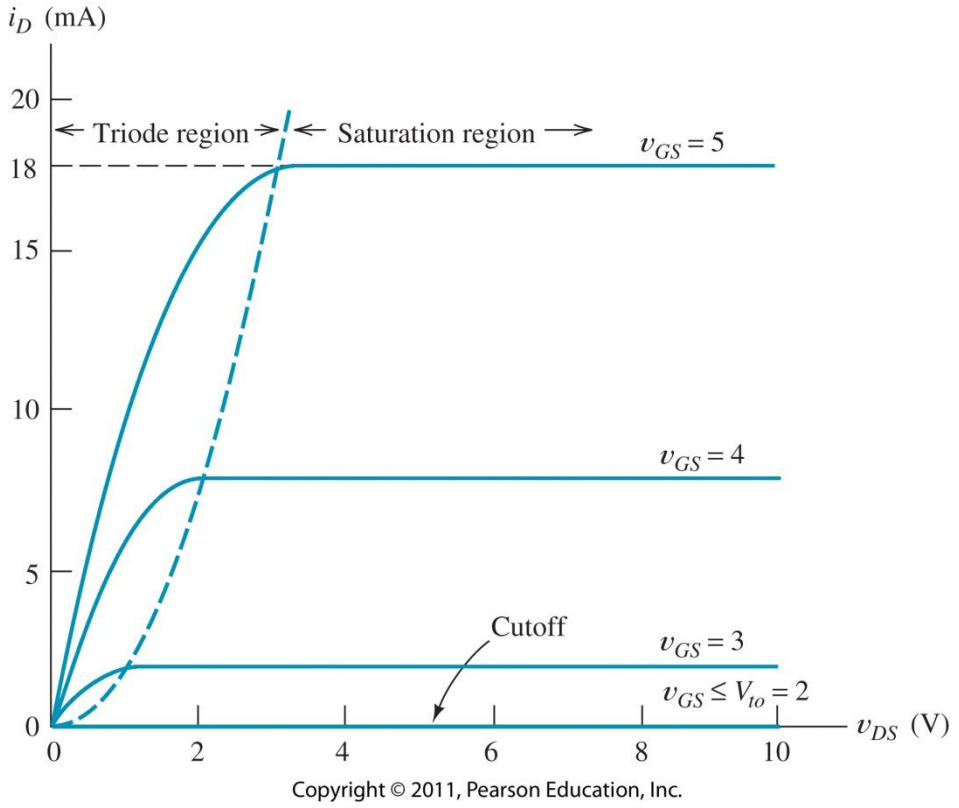




Transistor Operation

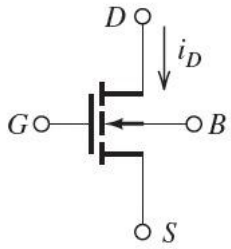
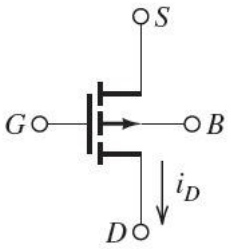
- Cutoff region
  - No drain current when gate voltage is below a threshold
  - $i_D = 0$ for $v_{GS} \leq V_{to}$
- Triode (linear) region
  - Transistor behaves like a resistor
  - $v_{DS} < v_{GS} - V_{to}$ and $v_{GS} \geq V_{to}$
- Saturation region
  - Constant current operation
  - $v_{DS} \geq v_{GS} - V_{to}$ and $v_{GS} \geq V_{to}$

- Above definitions for NMOS, PMOS has the same I/V characteristics but the signs of the voltages are inverted



MOSFET Summary

Table 12.1. MOSFET Summary

	NMOS	PMOS
Circuit symbol		
KP (typical value)	50 μA/V^2	25 μA/V^2
K	(1/2) KP (W/L)	(1/2) KP (W/L)
V_{to} (typical value)	+1 V	–1 V
Cutoff region	$v_{GS} \leq V_{to}$ $i_D = 0$	$v_{GS} \geq V_{to}$ $i_D = 0$
Triode region	$v_{GS} \geq V_{to}$ and $0 \leq v_{DS} \leq v_{GS} - V_{to}$ $i_D = K\,[2(v_{GS} - V_{to})\,v_{DS} - v_{DS}^2]$	$v_{GS} \leq V_{to}$ and $0 \geq v_{DS} \geq v_{GS} - V_{to}$ $i_D = K\,[2(v_{GS} - V_{to})\,v_{DS} - v_{DS}^2]$
Saturation region	$v_{GS} \geq V_{to}$ and $v_{DS} \geq v_{GS} - V_{to}$ $i_D = K\,(v_{GS} - V_{to})^2$	$v_{GS} \leq V_{to}$ and $v_{DS} \leq v_{GS} - V_{to}$ $i_D = K\,(v_{GS} - V_{to})^2$
v_{DS} and v_{GS}	Normally assume positive values	Normally assume negative values

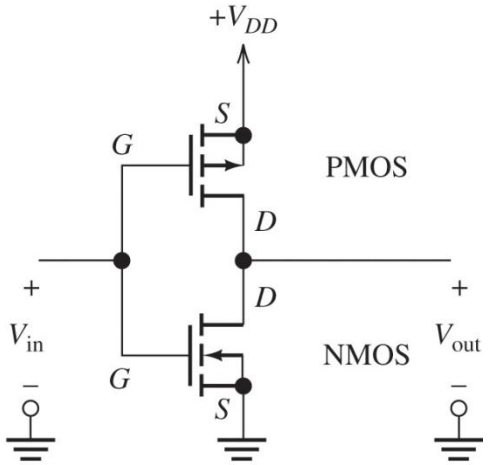
CMOS Logic Gates

- Logic gates composed of complementary metal-oxide semiconductor (CMOS) transistors
  - Both NMOS and PMOS transistors utilized in circuits
- With CMOS it is easy to build fundamental gates
  - E.g. NAND and NOR

- MOS operation is simplified with logic levels
  - The transistor is a voltage controlled switch
  - Either in cutoff or saturation
    - Cutoff = “off” = open switch
      - NMOS gate voltage low, PMOS gate voltage high
    - Saturation = “on” = closed switch
      - NMOS gate voltage high, PMOS gate voltage low

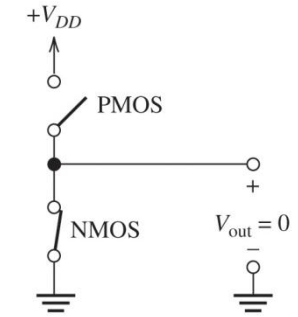
CMOS Inverter

- Stack a PMOS transistor above a NMOS transistor
- Tie gates together for the input



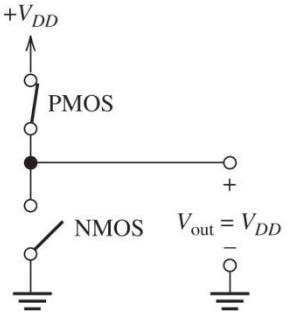
(b) Circuit diagram

- V_{in} high
  - V_{GS} NMOS: high → "on"
  - V_{GS} PMOS: low → "off"
  - V_{out} is low
    - Connection to ground



(c) Equivalent circuit with V_{in} high

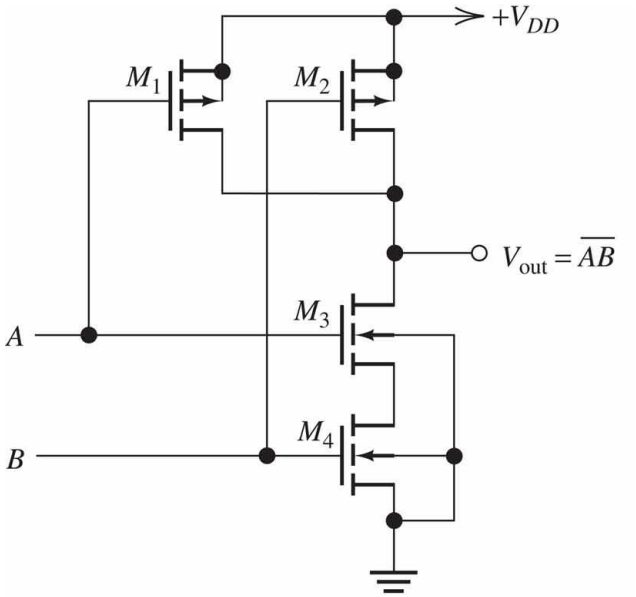
- V_{in} low
  - V_{GS} NMOS: low → "off"
  - V_{GS} PMOS: high → "on"
  - V_{out} is high
    - Connection to supply



(d) Equivalent circuit with V_{in} low

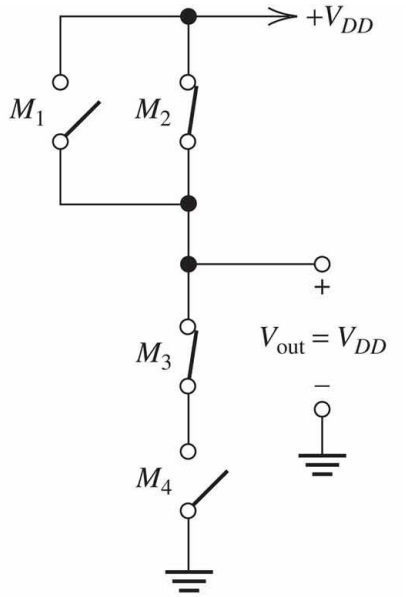
CMOS NAND Gate

- Parallel PMOS gates
- Stacked NMOS gates



(a) Circuit diagram

- *A* high and *B* low
  - NMOS on for high
  - PMOS on for low

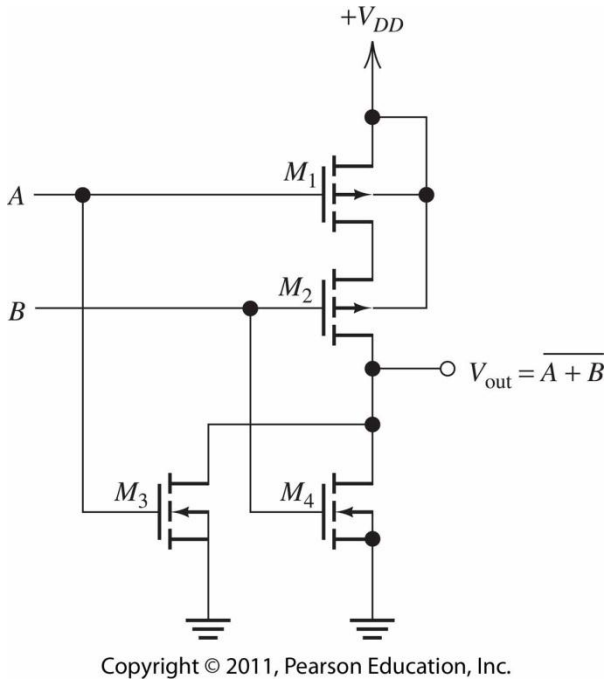


(b) *A* high and *B* low

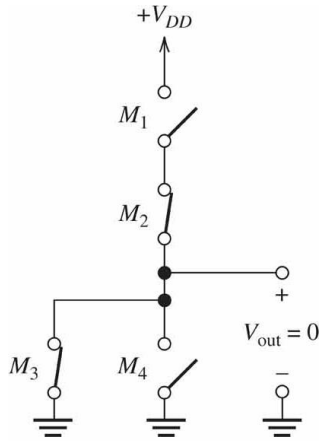
- Only PMOS path connected
  - V_{out} is high

CMOS NOR Gate

- Stacked PMOS gates
- Parallel NMOS gates



- *A* high and *B* low
  - NMOS on for high
  - PMOS on for low



(b) *A* high and *B* low

- Only NMOS path connected
  - V_{out} is low