EE292: Fundamentals of ECE

Fall 2012

TTh 10:00-11:15 SEB 1242

Lecture 25

121127

http://www.ee.unlv.edu/~b1morris/ee292/

Outline

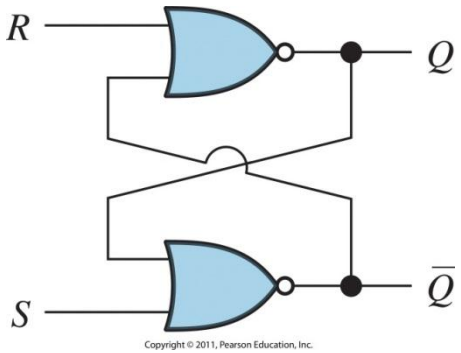
- Review
  - Sequential Logic
- Transistors
- CMOS Logic Gates

Sequential Logic

- Combinatorial logic output is only dependent on input at the given time
- Sequential logic has outputs that are dependent not only on current input but past input as well
  - The circuits have “memory”
- Often times sequential circuits use a clock signal to regulate when the output should change
  - These are called synchronous circuits
  - Asynchronous circuits are able to change as soon as inputs change (no clock signal is required)

SR Flip-Flop

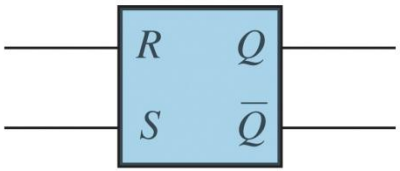
- This is the basic building block for sequential circuits
- A flip-flop has two allowable "states" of operation
  - It is able to store a bit of information
- It is a memory element because it stores a binary value
  - Coupled configuration ensures value Q does not change once set



- Set-reset (SR) flip-flop gives inputs to control the stored value Q
  - S = Set → $Q = 1$
  - R = Reset → $Q = 0$

R	S	Q_n
0	0	Q_{n-1}
0	1	1
1	0	0
1	1	Not allowed

(a) Truth table



(b) Circuit symbol

Clocked SR Flip-Flop

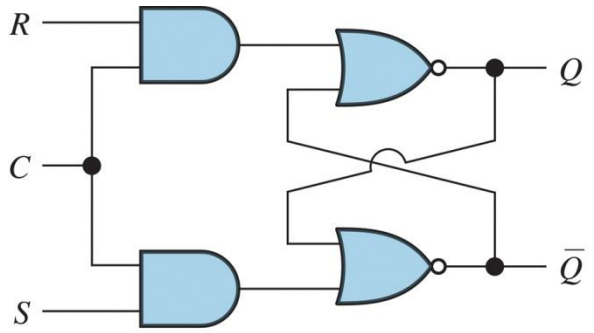
- Create a synchronous SR flip-flop to control the time when the output Q is allowed to change

- Add a clock signal to the flip-flop
  - Only when the clock is high is the output allowed to change

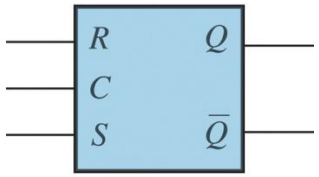
R	S	C	Q_n
0	0	×	Q_{n-1}
0	1	1	1
1	0	1	0
1	1	1	Not allowed
×	×	0	Q_{n-1}

(b) Truth table

- AND gates prevent R or S from reaching the flip-flop unless the clock C is high



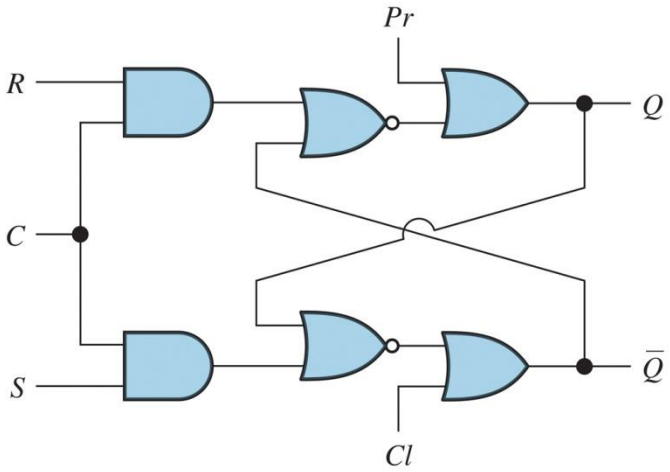
(a) Circuit diagram



(c) Circuit symbol

Clocked SR with Asynchronous Input

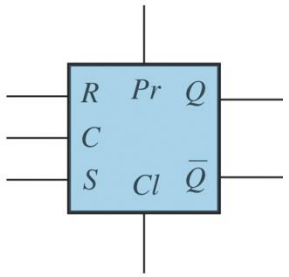
- Clocked set and reset functionality with asynchronous preset (Pr) and clear (Cl)



(a) Circuit diagram

Pr	Cl	R	S	C	Q_n
0	0	0	0	×	Q_{n-1}
0	0	0	1	1	1
0	0	1	0	1	0
×	×	1	1	1	Not allowed
0	1	×	×	×	0
1	0	×	×	×	1
1	1	×	×	×	Not allowed

(b) Truth table

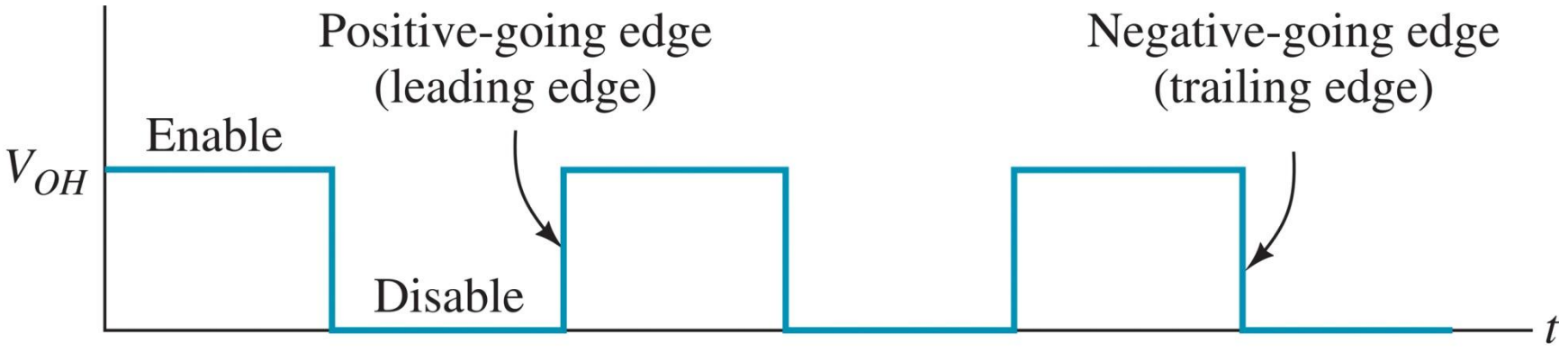


(c) Circuit symbol

- Add OR gates at $Q\bar{Q}$ outputs to automatically set or reset state
  - Notice that the clocked S and R cannot be high at the same time and neither can the asynchronous preset Pr and clear Cl

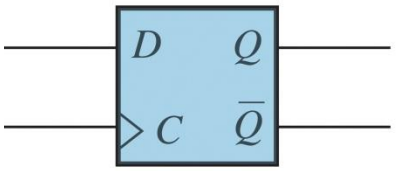
Edge-Triggered Circuits

- The clocked SR flip-flop uses the clock signal as an enable signal
  - When the clock is high the circuit is allowed to change
- Edge-triggered circuits only respond at the time when the clock changes between low and high
  - Positive-edge-triggered – low to high transition
    - Known as the leading edge
  - Negative-edge-triggered – high to low transition
    - Known as the training edge



D Flip-Flop

- The delay (D) flip-flop is edge-triggered to take make the output the same as the input right before the clock transition



(a) Circuit symbol

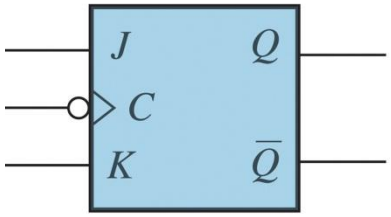
C	D	Q_n
0	×	Q_{n-1}
1	×	Q_{n-1}
↑	0	0
↑	1	1

(b) Truth table
indicates a transition
from low to high

- The triangle by the clock signal C indicates it is positive-edge-triggered
  - Up arrow in truth table indicates rising edge

JK Flip-Flop

- Similar operation to the SR flip-flop
  - Except when J and K are both high, the output state Q will toggle



(a) Circuit symbol

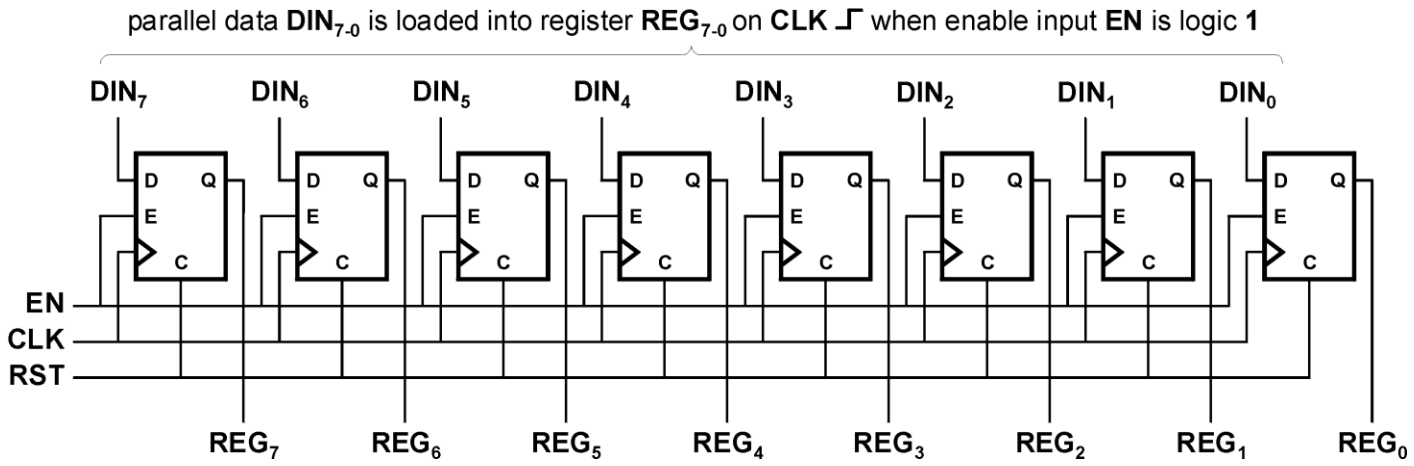
C	J	K	Q_n	Comment
0	×	×	Q_{n-1}	Memory
1	×	×	Q_{n-1}	Memory
↓	0	0	Q_{n-1}	Memory
↓	0	1	0	Reset
↓	1	0	1	Set
↓	1	1	$\overline{Q}_{n-1}$	Toggle

(b) Truth table indicates a transition from low to high

- Notice this is a negative-edge-triggered
  - Triangle with a preceding invert bubble

Registers

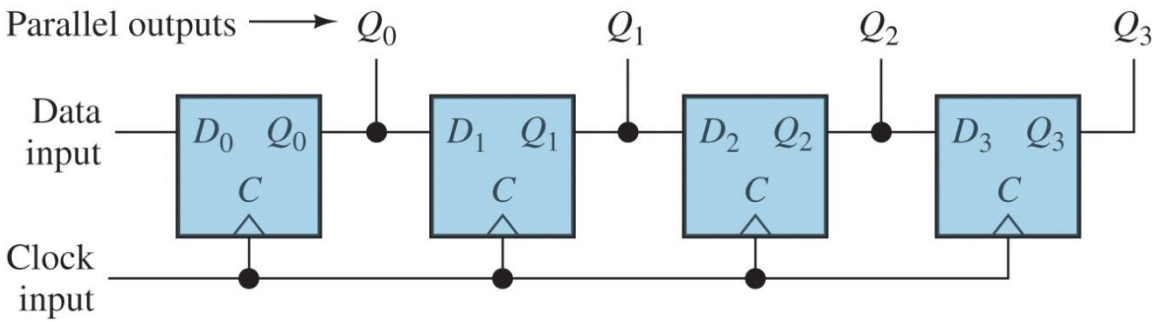
- A flip-flop is able to store a single bit
- A register is an array of flip-flops used to store a digital word
  - A hexadecimal number requires 4 bits so 4 flip-flops are required to internally store the hex number



http://enpub.fulton.asu.edu/cse517/Lab3.html

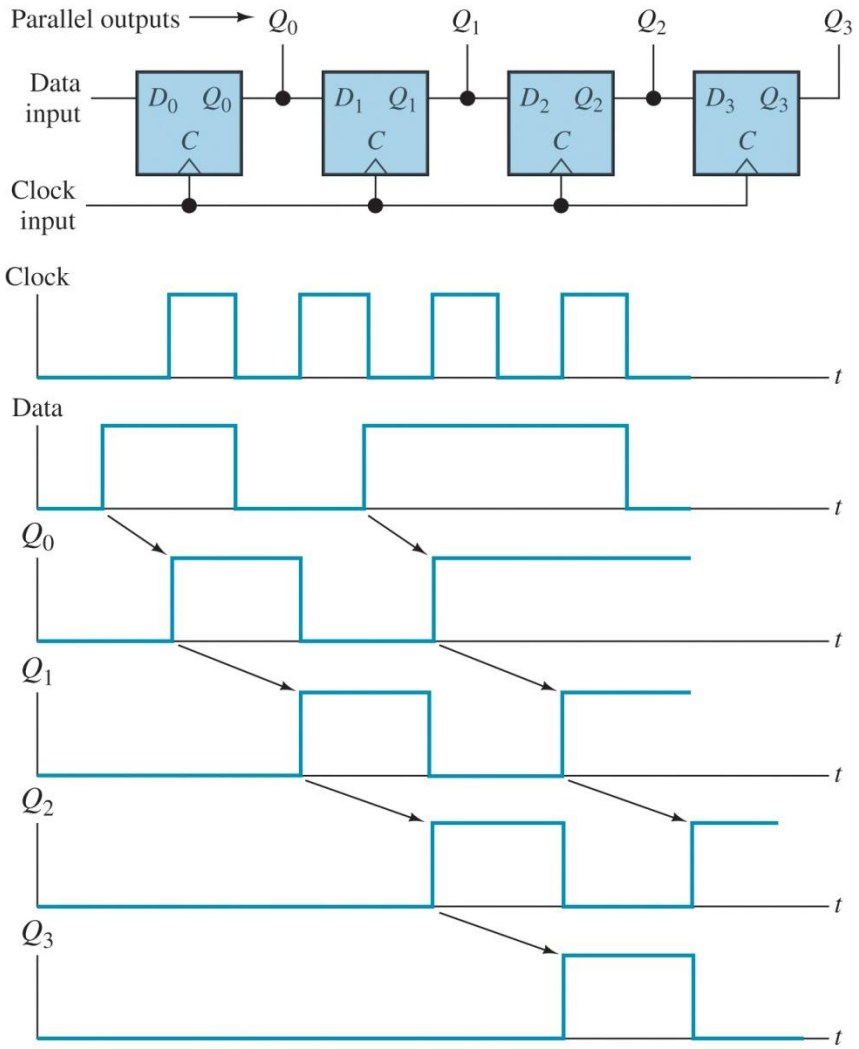
Serial-In Parallel-Out Shift Register

- Serial-in – implies bit are presented to the register one at a time (in a sequence)
- Parallel-out – implies the contents of the register (all the bits) can be accessed at the same time



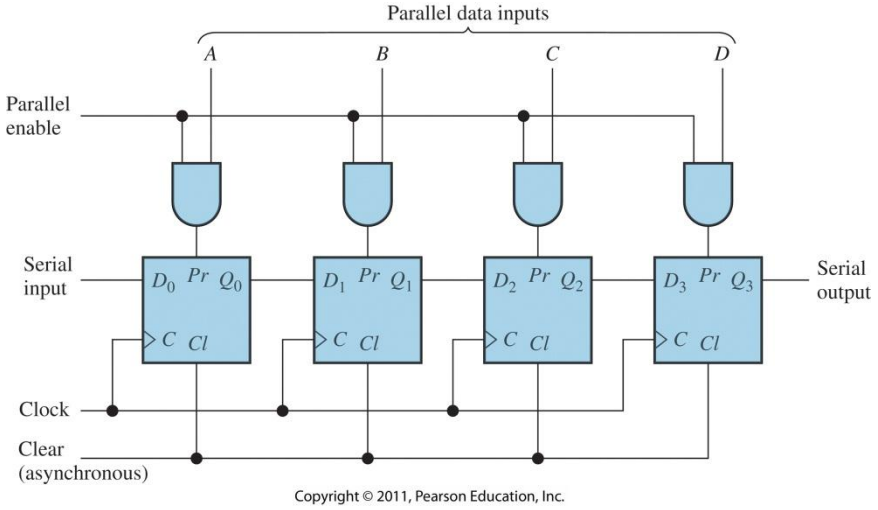
Serial-In Parallel-Out Operation

- Data is presented to a single input at the “front” of the word
- At each clock transition the data is shifted from one flip-flop to the next
- After 4 clock cycles, the full word is available to be read in the register



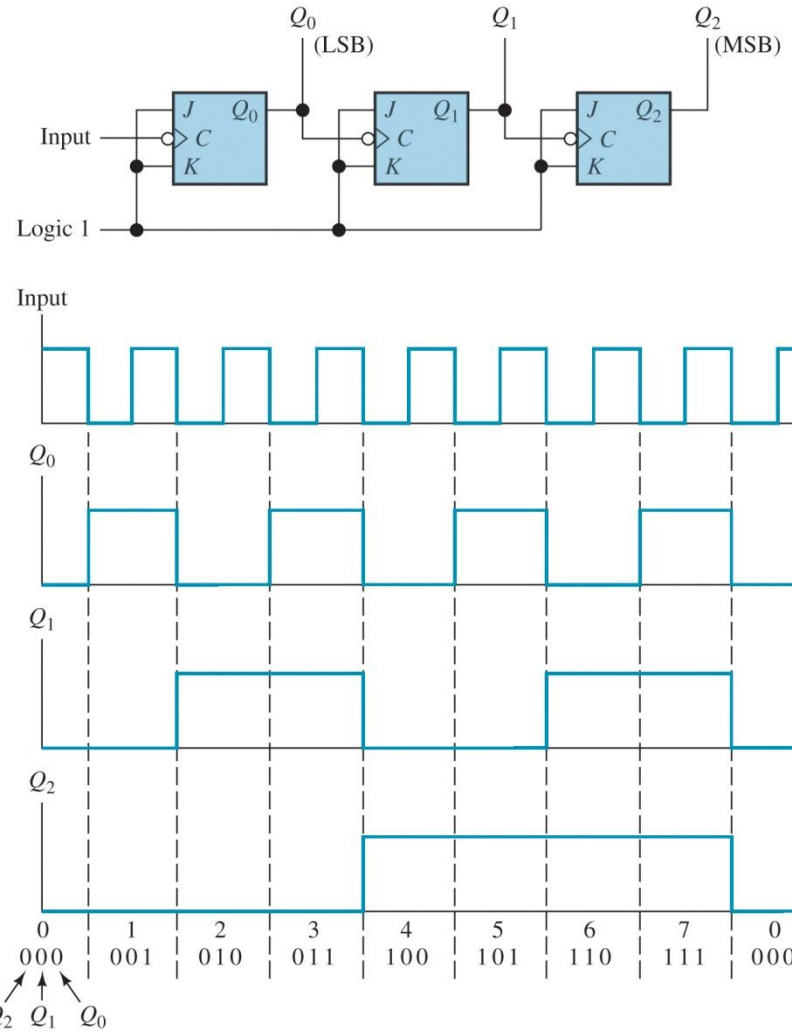
Parallel-In Serial Out Shift Register

- Parallel data is provided as input and the output is serial data
  - E.g. transmission of data on a telephone line
- The register can be cleared asynchronously to initialize the register
- Data is set on inputs and a parallel enable signal asynchronously loads the data
- The output is serially transmitted from the last flip-flop stage



Counters

- Circuit used to count the pulses in an input signal
  - Often the number of clocks are the signal of interest
- Inputs of JK flip-flop are tied together and high
  - Causes the output state to toggle with each clock cycle
  - Notice this is negative-edge-triggered
- Output of one JK flip-flop is the clock input of the next stage
  - The word $Q_2Q_1Q_0$ is the binary representation of the count



Minimization of Logic Circuits

- We saw you can minimize logic variable representations using Boolean algebra but this can be tedious and prone to error

- The Karnaugh map (K-map) (Ch 7.5) is a principled method for determining the minimum representation
  - This method is usually only practical for 4 variables (maybe 5 or 6)
  - We will not cover this in class but it is an interesting read

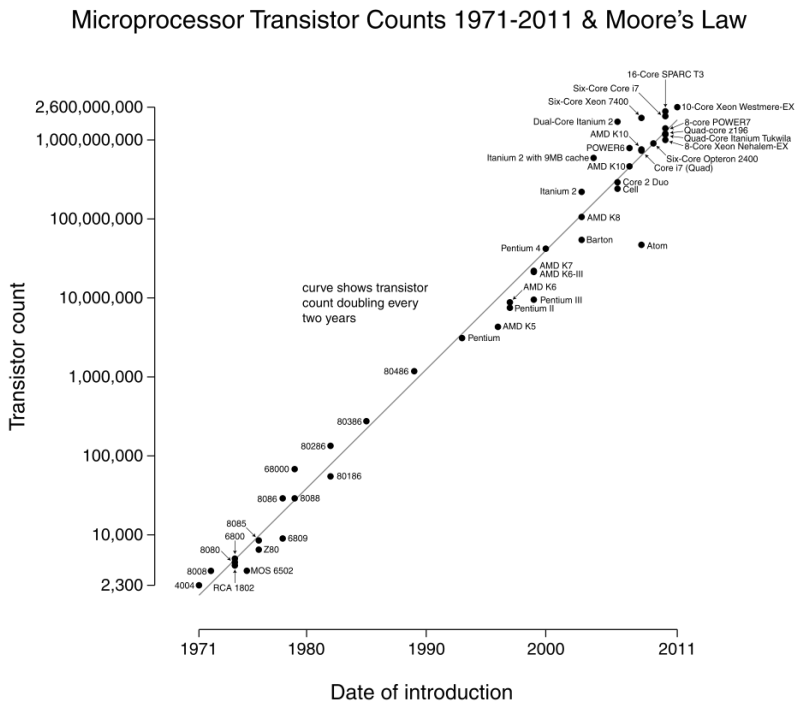
Transistor

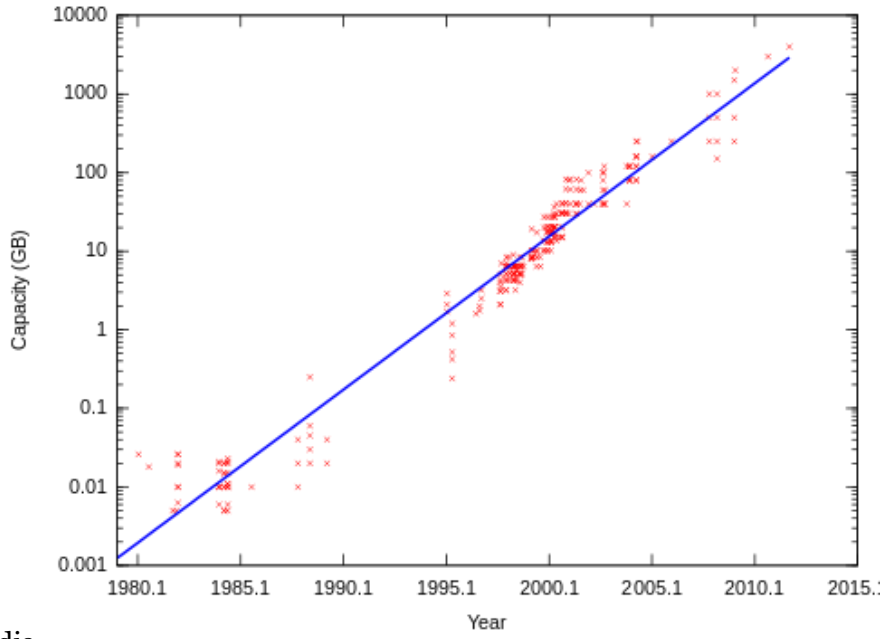
- Very important device used in amplifiers and logic gates
- Metal-oxide-semiconductor field-effect transistor (MOSFET) is the key device that has propelled our rapid technology growth
  - Can be easily fabricated on silicon wafers
  - Small area which enables large numbers of transistors on a chip and faster processing
  - Cheap

  - Insulated-gate field-effect transistor (IGFET) is the more general term for today's transistors

Moore's Law

- Observation by Intel co-founder Gordon E. Moore that the number of transistors on an integrated circuit doubles almost every two years (18 months)
- This exponential growth trend is also found in many areas of digital electronics
  - Processing speed, memory capacity, pixels in a digital camera, etc.

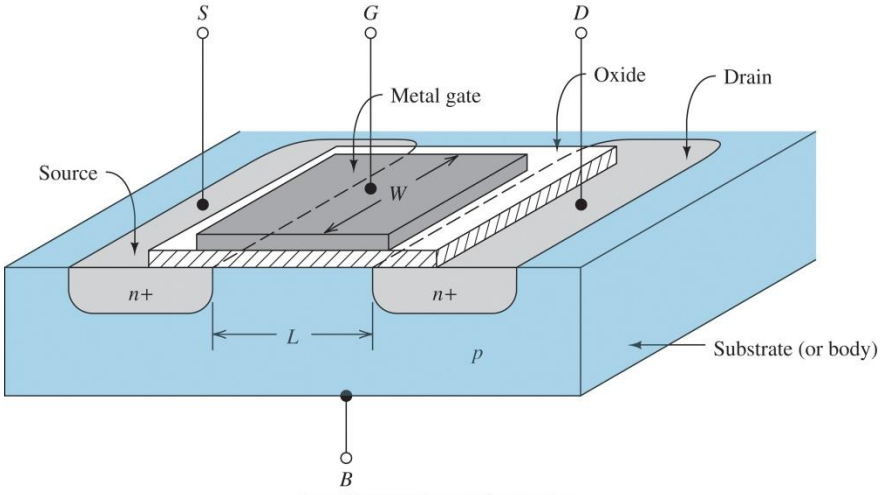




Wikipedia

Physical Transistor

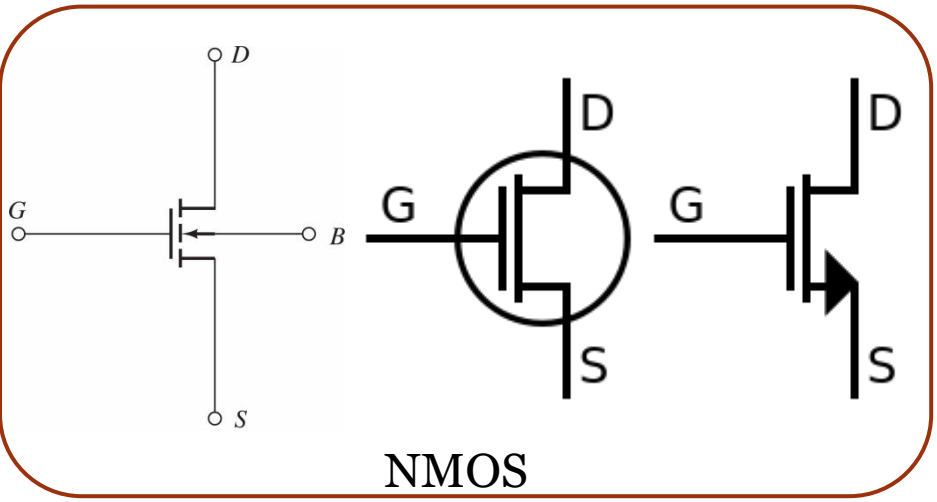
- A MOSFET transistor is a 4 terminal device that is fabricated on the surface of a silicon wafer
- 4 terminals
  - (D)rain
  - (G)ate
  - (S)ource
  - (B)ody or substrate
- Body is often tied to the source to make a 3 terminal device
- When voltage is applied on the gate and voltage is applied between the drain and source
  - Current flows into the drain and out the source terminal
  - Amount of current is controlled by the gate voltage

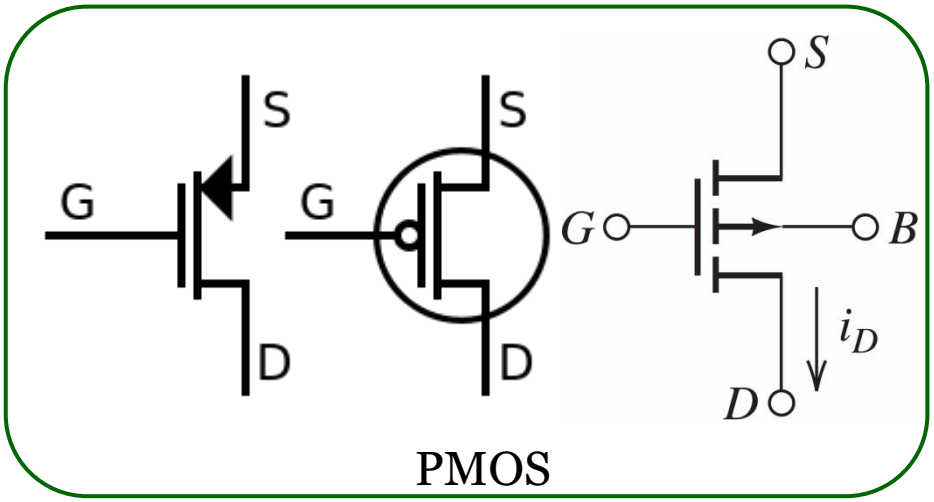


NMOS and PMOS Transistors

- NMOS
  - n-channel device → electrons carry charge into device
  - Current flows in from drain (out of source)
- Circuit symbol
  - Body arrow pointing to gate
  - Arrow pointing out from source

- PMOS
  - p-channel device → "holes" carry positive charge
  - Current flows out of drain (in from source)
- Circuit symbol
  - Body arrow pointing away from gate
  - Arrow pointing in from source
  - Invert bubble on the gate

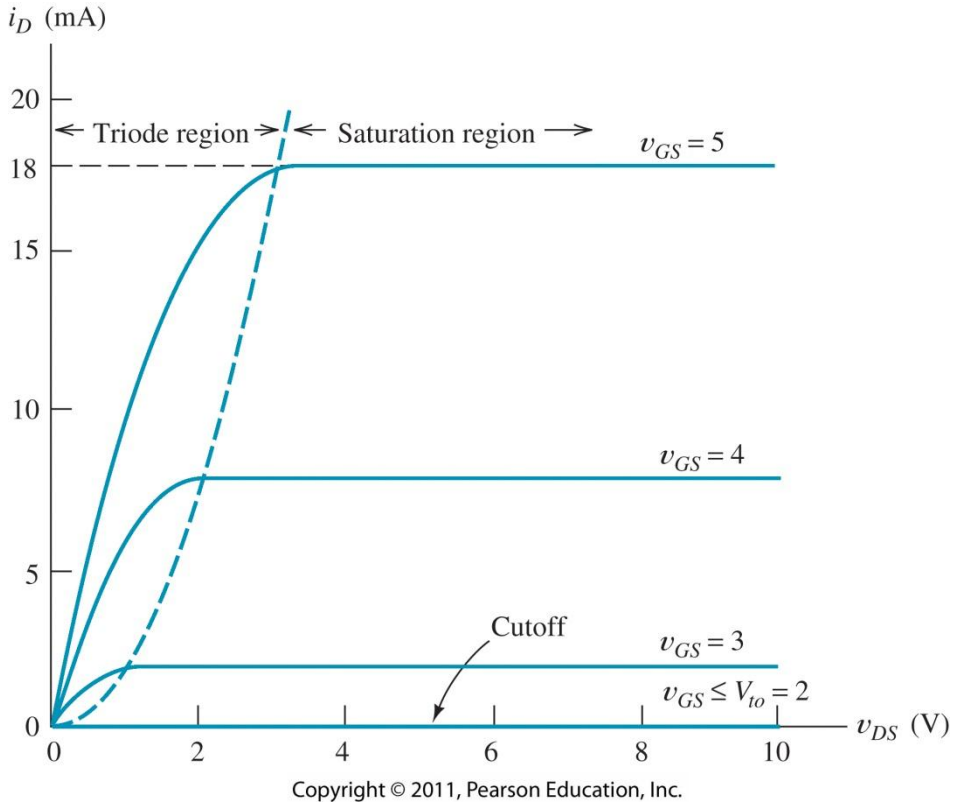




Transistor Operation

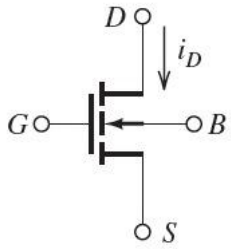
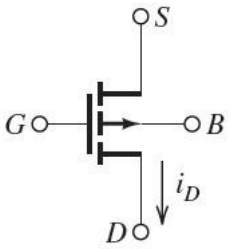
- Cutoff region
  - No drain current when gate voltage is below a threshold
  - $i_D = 0$ for $v_{GS} \leq V_{to}$
- Triode (linear) region
  - Transistor behaves like a resistor
  - $v_{DS} < v_{GS} - V_{to}$ and $v_{GS} \geq V_{to}$
- Saturation region
  - Constant current operation
  - $v_{DS} \geq v_{GS} - V_{to}$ and $v_{GS} \geq V_{to}$

- Above definitions for NMOS, PMOS has the same I/V characteristics but the signs of the voltages are inverted



MOSFET Summary

Table 12.1. MOSFET Summary

	NMOS	PMOS
Circuit symbol		
KP (typical value)	50 μA/V^2	25 μA/V^2
K	(1/2) KP (W/L)	(1/2) KP (W/L)
V_{to} (typical value)	+1 V	–1 V
Cutoff region	$v_{GS} \leq V_{to}$ $i_D = 0$	$v_{GS} \geq V_{to}$ $i_D = 0$
Triode region	$v_{GS} \geq V_{to}$ and $0 \leq v_{DS} \leq v_{GS} - V_{to}$ $i_D = K\,[2(v_{GS} - V_{to})\,v_{DS} - v_{DS}^2]$	$v_{GS} \leq V_{to}$ and $0 \geq v_{DS} \geq v_{GS} - V_{to}$ $i_D = K\,[2(v_{GS} - V_{to})\,v_{DS} - v_{DS}^2]$
Saturation region	$v_{GS} \geq V_{to}$ and $v_{DS} \geq v_{GS} - V_{to}$ $i_D = K\,(v_{GS} - V_{to})^2$	$v_{GS} \leq V_{to}$ and $v_{DS} \leq v_{GS} - V_{to}$ $i_D = K\,(v_{GS} - V_{to})^2$
v_{DS} and v_{GS}	Normally assume positive values	Normally assume negative values

MOSFETs for Amplifiers

- Must bias the FET into a particular region of operation
  - DC bias of circuit
- Small signal analysis is used to describe how current and voltage change around the DC operating point
  - Used to design amplifiers that magnify small changes of input voltage (current) into large changes in output voltage (current)

- We will not study how to do this in our class

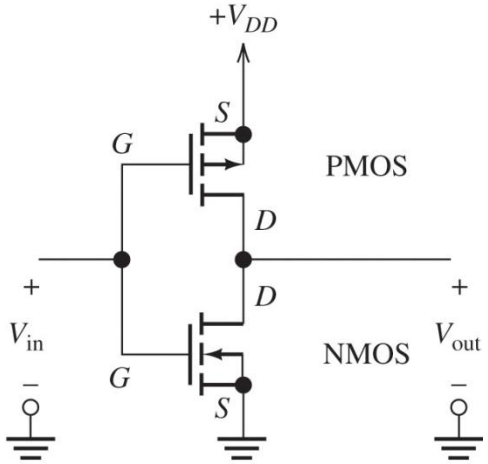
CMOS Logic Gates

- Logic gates composed of complementary metal-oxide semiconductor (CMOS) transistors
  - Both NMOS and PMOS transistors utilized in circuits
- With CMOS it is easy to build fundamental gates
  - E.g. NAND and NOR

- MOS operation is simplified with logic levels
  - The transistor is a voltage controlled switch
  - Either in cutoff or saturation
    - Cutoff = “off” = open switch
    - Saturation = “on” = closed switch

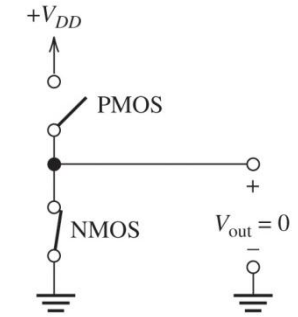
CMOS Inverter

- Stack a PMOS transistor above a NMOS transistor
- Tie gates together for the input



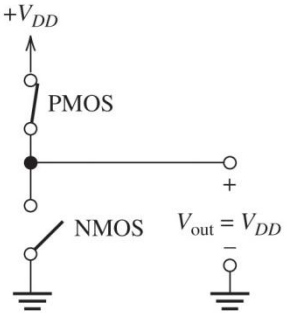
(b) Circuit diagram

- V_{in} high
  - V_{GS} NMOS: high → "on"
  - V_{GS} PMOS: low → "off"
  - V_{out} is low
    - Connection to ground



(c) Equivalent circuit with V_{in} high

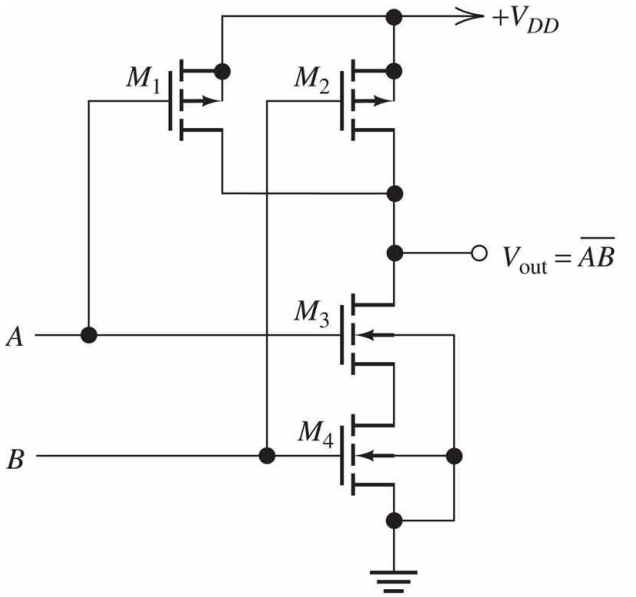
- V_{in} low
  - V_{GS} NMOS: low → "off"
  - V_{GS} PMOS: high→ "on"
  - V_{out} is high
    - Connection to supply



(d) Equivalent circuit with V_{in} low

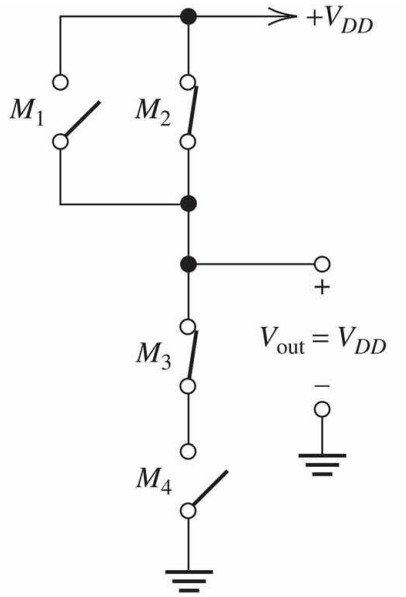
CMOS NAND Gate

- Parallel PMOS gates
- Stacked NMOS gates



(a) Circuit diagram

- *A* high and *B* low
  - NMOS on for high
  - PMOS on for low

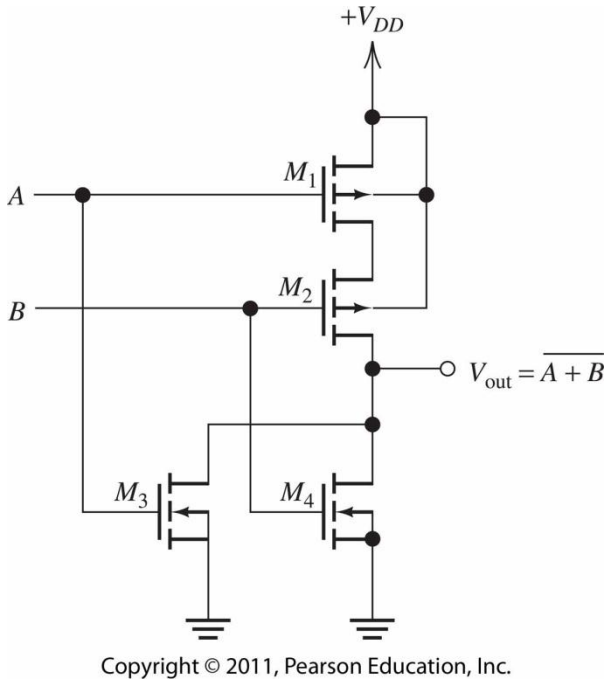


(b) *A* high and *B* low

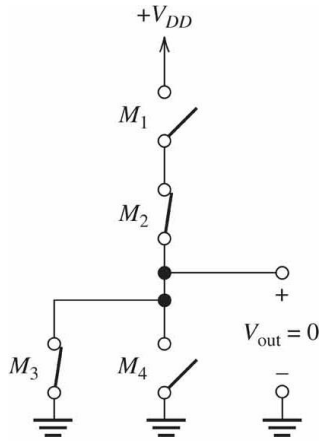
- Only PMOS path connected
  - V_{out} is high

CMOS NOR Gate

- Stacked PMOS gates
- Parallel NMOS gates



- *A* high and *B* low
  - NMOS on for high
  - PMOS on for low



(b) *A* high and *B* low

- Only NMOS path connected
  - V_{out} is low