

Homework #8
No Due Date

1. (H&J 7.10)
A $256\text{ M} \times 1$ dynamic RAM, organized as a $16,384 \times 16,384$ cell array, must be refreshed every 13 ms. If RAS-only refresh is employed, and $t_C = 50\text{ ns}$, what is the minimum percentage of time that must be devoted to refreshing the chip?
2. (H&J 7.19)
A certain two-way set-associative cache has an access time of 4 ns, compared to a miss time of 60 ns. Without the cache, main memory access time was 50 ns. Running a set of benchmarks with and without the cache indicated a speedup of 90%. What is the approximate hit ratio?
3. (H&J 7.20)
A 128 MB main memory has 64 KB direct-mapped cache with 16 bytes per line.
 - (a) How many lines are there in the cache?
 - (b) Show how the main memory address is partitioned?
4. (H&J 7.21)
A certain memory system has a 128 MB main memory and a 2 MB cache. Blocks are 32 bytes in size. Show the fields in a memory address if the cache is
 - (a) associative
 - (b) direct-mapped
 - (c) 8-way set-associative
5. (H&J 7.25)
A disk has an average seek time of 7 ms and an average rotational latency of 8.3 ms. Its transfer rate is 54 MB/s. What size block is necessary so that delay in locating the data is only 50% of the total time to read or write a block? Discuss whether all of a virtual memory page of this size would be likely to be accessed in main memory before it is replaced. See the discussion of disk organization on page 411 for a description of disk properties.