

Homework #5  
Due Mon. 11/02

1. (H&J 4.1)  
Write the concrete RTN steps for the SRC instructions `la` and `st r` using the 1-bus SRC microarchitecture of Section 4.2.
2. (H&J 4.2)  
Extend the SRC instruction set by adding the instruction `swap ra, rb`, (`op=7`), that exchanges the contents of the two specified registers.
  - (a) Define a plausible abstract RTN for this instruction.
  - (b) Develop the concrete RTN for it, assuming the 1-bus SRC microarchitecture.
3. (H&J 4.4)  
Extend the SRC instruction set by adding the `xor` command, (`op=19`), which is similar to the `and` command, but performs the XOR operation instead of AND.
  - (a) Develop the abstract RTN for the `xor` command.
  - (b) Write the concrete RTN and control signals for the `xor` instruction for the 1-bus SRC microarchitectue. (Unfortunately, the SRC ALU does not have the XOR operation as one of its primitives, but only the operations ADD, SUB, AND, OR, SHR, SHL, NEG, NOT, C=B, and INC4).
4. (H&J 4.5)  
Write concrete RTN steps and control sequences for the `not` instruction implemented in the 1-bus microarchitecture.
5. (H&J 4.6)  
Why, in Figure 4.8 does the C=B signal not have to be asserted when that operation is to be performed?
6. (H&J 4.13)  
The 2-bus SRC design shown in Figure 4.16 allows savings in the number of control steps to perform an `add` instruction, but at the expense of additional control hardware. The text describes the need to provide additional gate and strobe hardware so that data can be gated from and strobed to the general registers on the same cycle. Redesign the hardware shown in Figure 4.4 to accommodate this change.
7. (H&J 4.15)  
Repeat Exercise 4.5 for the 2- and 3-bus microarchitectures.
8. (H&J 4.19)  
Design a new opcode for SRC, `reset`, (`op=18`), that does a hard reset or a soft reset, depending on the value of `c1<0`.
9. (H&J 4.22)  
In most cases, an interrupted program must be resumed after the exception that interrupted it has been handled. In some cases, however, the nature of the exception precludes resuming the program. Identify the two different kinds of exceptions of those discussed in Section 4.8.2.