Timing

• Flip-flop samples $D$ at clock edge
• $D$ must be stable when sampled
  • Similar to a photograph, $D$ must be stable around clock edge
  • Moving right before or after shutter click results in blurry photo
• If not, metastability can occur
Input Timing Constraints

- **Setup time**: $t_{\text{setup}} = \text{time before clock edge data must be stable (i.e. not changing)}$
- **Hold time**: $t_{\text{hold}} = \text{time after clock edge data must be stable}$
- **Aperture time**: $t_a = \text{time around clock edge data must be stable} \ (t_a = t_{\text{setup}} + t_{\text{hold}})$
Output Timing Constraints

- **Propagation delay:** $t_{pcq} = \text{time after clock edge that the output } Q \text{ is guaranteed to be stable (i.e., to stop changing)}$
- **Contamination delay:** $t_{ccq} = \text{time after clock edge that } Q \text{ might be unstable (i.e., start changing)}$
Dynamic Discipline

• Synchronous sequential circuit inputs must be stable during aperture (setup and hold) time around clock edge
  • Specifically, inputs must be stable:
    • at least $t_{\text{setup}}$ before the clock edge
    • at least until $t_{\text{hold}}$ after the clock edge

• Previously, static discipline:
  • With logically valid inputs, every circuit element must produce logically valid outputs
• The delay between registers has a minimum and maximum delay, dependent on the delays of the circuit elements.

Dynamic Discipline
• Depends on the **maximum** delay from register R1 through combinational logic to R2
• The input to register R2 must be stable at least $t_{\text{setup}}$ before clock edge

\[ T_c \geq \]
Setup Time Constraint

- Depends on the **maximum** delay from register R1 through combinational logic to R2
- The input to register R2 must be stable at least $t_{\text{setup}}$ before clock edge

$$T_c \geq t_{pcq} + t_{pd} + t_{\text{setup}}$$

$t_{pd} \leq$
Setup Time Constraint

- Depends on the maximum delay from register R1 through combinational logic to R2
- The input to register R2 must be stable at least $t_{\text{setup}}$ before clock edge

$$T_c \geq t_{pcq} + t_{pd} + t_{\text{setup}}$$

$t_{pd} \leq T_c - (t_{pcq} + t_{\text{setup}})$

$(t_{pcq} + t_{\text{setup}})$: sequencing overhead
Hold Time Constraint

- Depends on the **minimum** delay from register R1 through the combinational logic to R2
- The input to register R2 must be stable for at least $t_{\text{hold}}$ after the clock edge

![Diagram of hold time constraint]

\[ t_{\text{hold}} < \]
Hold Time Constraint

- Depends on the **minimum** delay from register R1 through the combinational logic to R2.
- The input to register R2 must be stable for at least $t_{\text{hold}}$ after the clock edge.

\[
t_{\text{hold}} < t_{\text{ccq}} + t_{\text{cd}}
\]

$t_{cd} >$
Hold Time Constraint

- Depends on the **minimum** delay from register R1 through the combinational logic to R2
- The input to register R2 must be stable for at least $t_{\text{hold}}$ after the clock edge

\[
t_{\text{hold}} < t_{\text{ccq}} + t_{\text{cd}}
\]
\[
t_{\text{cd}} > t_{\text{hold}} - t_{\text{ccq}}
\]
Timing Analysis

Timing Characteristics

- $t_{ccq} = 30$ ps
- $t_{pcq} = 50$ ps
- $t_{setup} = 60$ ps
- $t_{hold} = 70$ ps
- $t_{pd} = 35$ ps
- $t_{cd} = 25$ ps

Setup time constraint:

$T_c \geq \bar{t}_{ccq} + t_{cd}$

Hold time constraint:

$t_{ccq} + t_{cd} > t_{hold}$?
### Timing Analysis

#### Timing Characteristics

- $t_{ccq} = 30$ ps
- $t_{pcq} = 50$ ps
- $t_{setup} = 60$ ps
- $t_{hold} = 70$ ps
- $t_{pd} = 35$ ps per gate
- $t_{cd} = 25$ ps

#### Setup time constraint:

$$T_c \geq (50 + 105 + 60) \text{ ps} = 215 \text{ ps}$$

$$f_c = \frac{1}{T_c} = 4.65 \text{ GHz}$$

#### Hold time constraint:

$$t_{ccq} + t_{cd} > t_{hold} ?$$

$$(30 + 25) \text{ ps} > 70 \text{ ps} ? \text{ No!}$$
Timing Analysis

Add buffers to the short paths:

```
CLK
| A
| B
| C
| D

CLK
| X'
| Y'

CLK
| X
| Y
```

Timing Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{ccq}$</td>
<td>30 ps</td>
</tr>
<tr>
<td>$t_{pcq}$</td>
<td>50 ps</td>
</tr>
<tr>
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</tr>
</tbody>
</table>

Setup time constraint:

$$T_c \geq$$

$T_c$ =

Hold time constraint:

$$t_{ccq} + t_{cd} > t_{hold} ?$$

$t_{ccq}$ = 30 ps
$t_{pcq}$ = 50 ps
$t_{setup}$ = 60 ps
$t_{hold}$ = 70 ps

Add buffers to the short paths:

$t_{pd} =$
$t_{cd} =$

Setup time constraint:

$$T_c \geq$$

$T_c$ =

Hold time constraint:

$$t_{ccq} + t_{cd} > t_{hold} ?$$
Add buffers to the short paths:

Timing Characteristics:

- \( t_{ccq} = 30 \text{ ps} \)
- \( t_{pcq} = 50 \text{ ps} \)
- \( t_{setup} = 60 \text{ ps} \)
- \( t_{hold} = 70 \text{ ps} \)
- \( t_{pd} = 35 \text{ ps} \) per gate
- \( t_{cd} = 25 \text{ ps} \) per gate

Setup time constraint:

\[ T_c \geq (50 + 105 + 60) \text{ ps} = 215 \text{ ps} \]

\[ f_c = \frac{1}{T_c} = 4.65 \text{ GHz} \]

Hold time constraint:

\[ t_{ccq} + t_{cd} > t_{hold} ? \]

\[ (30 + 50) \text{ ps} > 70 \text{ ps} ? \quad \text{Yes!} \]