Homework #9
Due Su. 11/27

Note: Do not use a calculator or computer to complete the following exercises. You must show all your work and put a box around your final answer to receive credit. Messy or unreadable submissions will receive no credit.

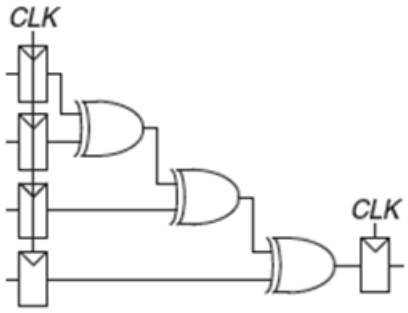
Homework will only be accepted at the beginning of class and all pages must be stapled together.

Total Points: 121

1. (0 points) How long did it take you to complete the homework? This will not affect your grade (unless omitted) but it helps gauge the workload for this and future semesters. If you do not answer this question you will get -5 points.

2. (30 points) Timing Analysis

   Consider the circuit below that computes a registered four-input XOR function. Each two-input XOR gate has a propagation delay of 100 ps and a contamination delay of 55 ps. Each flip-flop has a setup time of 60 ps, a hold time of 20 ps, a clock-to-Q maximum delay of 70 ps, and a clock-to-Q minimum delay of 50 ps.



   (a) (6 points) What is the minimum cycle time of the system?

   (b) (6 points) What is the maximum operating frequency of the system?

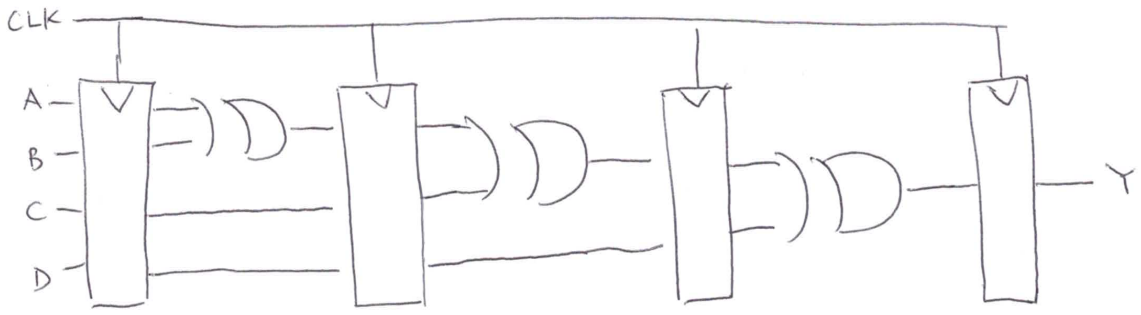
   (c) (6 points) Is the hold time constraint violated? Justify your answer.

   (d) (6 points) What is the latency of the circuit (i.e. the time to make a single 4-input XOR calculation)? The answer should be in ps.

   (e) (6 points) What is the throughput of the circuit (i.e. how many 4-input XOR calculations are completed per second)? The answer should be in # calculations/second.

3. (36 points) Temporal Parallelism (Pipelining)

   You implement the four-input XOR function using temporal parallelism (pipelining) by adding a register between the input and output of each XOR gate as shown in the circuit below. Each two-input XOR gate has a propagation delay of 100 ps and a contamination delay of 55 ps. Each flip-flop has a setup time of 60 ps, a hold time of 20 ps, a clock-to-Q maximum delay of 70 ps, and a clock-to-Q minimum delay of 50 ps.



(a) (6 points) What is the minimum cycle time of the system?

(b) (6 points) What is the maximum operating frequency of the system?

(c) (6 points) Is the hold time constraint violated? Justify your answer.

(d) (6 points) What is the latency of the circuit (i.e. the time to make a single 4-input XOR calculation)? The answer should be in ps.

(e) (6 points) What is the throughput of the circuit (i.e. how many 4-input XOR calculations are completed per second)? The answer should be in # calculations/second.

(f) (6 points) Compare this circuit to the the one from Question 2. Discuss advantages and disadvantages.

4. (55 points) FSM: 1965 Ford Thunderbird Tail Lights Computer Assignment

   Full instructions on the website

   `http://www.ee.unlv.edu/~b1morris/cpe100/docs/comp03.pdf`.

   (a) (0 points) How many hours did you spend on the lab?

   (b) (10 points) Full FSM design, including a completed state transition diagram for your FSM and schematic.

   (c) (20 points) A printout of the Quartus II schematic.

   (d) (20 points) A print out of the ModelSim simulation of the circuit. Make sure you test the circuit completely. Show the result for a reset, left signal, and right signal. Your signals should be printed in the following order: $clk, reset, left, right, LC, LB, LA, RA, RB, RC$.

   (e) (5 points) A brief paragraph (2-4 sentences) highlighting what you learned on this lab assignment. List any difficulties you encountered.

5. (0 points) Teaching Evaluation

   Reminder, you should have received an email to your RebelMail account asking to give an evaluation of the course. Please do take the ~ 3 minutes required to enter in your assessment. This provides feedback which is helpful for improving further iterations of the course.