Professor Brendan Morris, SEB 3216, brendan.morris@unlv.edu

CPE100: Digital Logic Design I

Introduction

http://www.ee.unlv.edu/~b1morris/cpe100/

Class Website

- http://www.ee.unlv.edu/~b1morris/cpe100/

- This will have the most up-to-date information about the class.
  - Weekly schedule
  - Tentative dates for exams
  - Homework assignments (first one posted already)

- Syllabus
  - Full course description online
  - http://www.ee.unlv.edu/~b1morris/cpe100/docs/syllabus.pdf

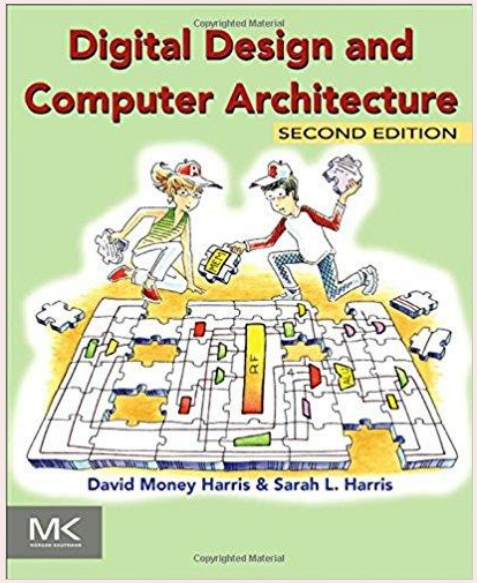
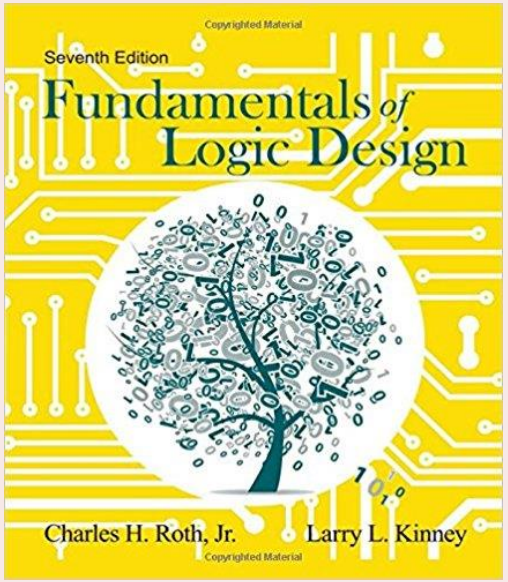
Instructor

- Dr. Brendan Morris
- Office: SEB 3216 (see reception desk)
- Office Hours (tentative)
  - MW 16:00-17:00 and TTh 12:00-13:00
  - Email for appointments at other times
  - Poll:
    - Office hours work?

Important Dates

- Lecture
  - TuTh 13:00-14:15, SEB 1242
- Final
  - Tu/Th Dec. 10/12, 13:00-15:00
  - Look up your final exam schedule now to determine conflicts. I must be notified within the first month or I will not be able to help
- Midterms (tentative)
  - 10/03, 11/14

Textbook

Required	Recommended Reading
Digital Design and Computer Architecture, Harris and Harris, 2nd Edition ISBN: 978-0123944245	Fundamentals of Logic Design, Roth and Kinney, 7th Edition ISBN: 978-1133628477
	
[1st Ed. link] for reference only	

Grading

- Midterms: 40%
- Final: 25%
- Homework: 25%
- Participation: 10%

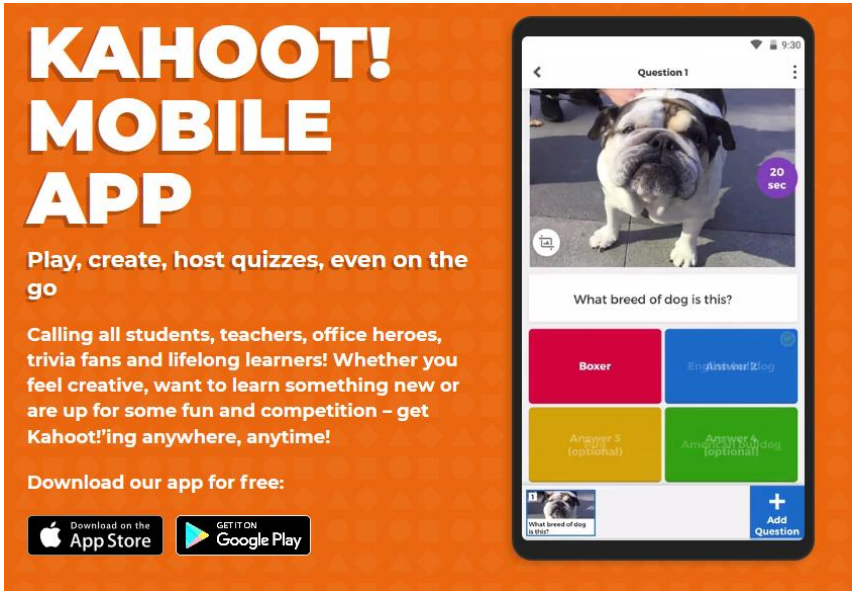
- Homework will include logic design software to build and test digital circuits. Students may work together in study groups but all assignments must be completed individually.

- Homework will be due at the beginning of class on the designated date. No late homework will be accepted unless prior notification and arrangements are made.

- As a university student it is your responsibility to conduct yourself ethically and with integrity as described in the Academic misconduct Policy. Cheating and plagiarism will not be tolerated. Any student caught cheating will be given an F grade. (http://studentconduct.unlv.edu/misconduct/policy.html)

Participation

- Will be tracked using online framework
  - https://kahoot.it/
  - Download App here
- Must have access to smart phone or web connected device
- In-class questions do not require sign-up but you must use your Webcampus (ACE) account to be properly tracked



Catalog Description

- Logic gates. Simplification of Boolean functions. Design and testing of combinational and sequential circuits including code converters, multiplexers, adders, and synchronous counters.

- Prerequisites
  - MATH 127 OR MATH 128 OR MATH 181 OR higher, OR SAT math score of 630 or higher OR ACT math score of 28 or higher. MATH 127 or MATH 128 must be completed with a grade of C or better

Tips for Success

- **Participate**: Attend class and take part in discussion.
- **Practice**: Spend ample time on homework.
- **Question**: Do not be afraid to ask questions.
- **Network**: Find people taking the same courses as you and build study groups.
- **Review**: Don't just do what is asked in class.
- **Be RESPONSIBLE**: You are an adult and must be responsible for your academic career.

Questions?